

230667 - SCPD - System on Chip Physical Design

Coordinating unit:	230 - ETSETB - Barcelona School of Telecommunications Engineering
Teaching unit:	710 - EEL - Department of Electronic Engineering
Academic year:	2017
Degree:	DEGREE IN ELECTRONIC ENGINEERING (Syllabus 1992). (Teaching unit Optional) MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2009). (Teaching unit Optional) MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2013). (Teaching unit Optional)
ECTS credits:	5
Teaching languages:	English

Teaching staff

Coordinator:	Moll Echeto, Francesc De Borja Rubio Sola, Jose Antonio
Others:	Moll Echeto, Francesc De Borja Rubio Sola, Jose Antonio

Opening hours

Timetable:	6 hours per week
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Prior skills

Basic knowledge of CMOS technology and design.
Basic knowledge of digital design, combinational and sequential.

Requirements

Graduate studies in Electronic Engineering or equivalent

Degree competences to which the subject contributes

Specific:

- CEE18. Ability to design CMOS digital and analog integrated circuits of medium complexity.
- CEE19. Ability to apply low-power techniques to integrated circuits (ICs).

Transversal:

1. **TEAMWORK:** Being able to work in an interdisciplinary team, whether as a member or as a leader, with the aim of contributing to projects pragmatically and responsibly and making commitments in view of the resources that are available.
2. **EFFECTIVE USE OF INFORMATION RESOURCES:** Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.
3. **FOREIGN LANGUAGE:** Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

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Teaching methodology

- Lectures
- Laboratory activities
- Individual work
- Short answer test and exercises (Final Exam)

Learning objectives of the subject

Learning objectives of the subject:

The aim of this course is to train students in methods of design of CMOS integrated circuits from a high level description to a layout in an efficient way using computers so that the resulting layout satisfies topological, geometric, timing and power-consumption constraints of the design.

Learning results of the subject:

- Ability to understand and apply timing and power constraints to a complex integrated circuit.
- Ability to perform the physical implementation of a complex integrated circuit.
- Ability to apply low power design techniques to integrated circuit design.
- Ability to develop techniques for the design, analysis and evaluation of electronic systems in applications such as automation, aerospace, energy distribution and generation, consumer electronics, biomedicine, etc.
- Ability to analyze, design and evaluate microelectronic integrated circuits.
- Ability to implement advanced design techniques of microelectronic integrated circuits.
- Ability to use state of the art computer aided design (CAD) tools for the design of integrated circuits.

Study load

Total learning time: 125h	Hours large group:	13h	10.40%
	Hours medium group:	0h	0.00%
	Hours small group:	26h	20.80%
	Guided activities:	0h	0.00%
	Self study:	86h	68.80%

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Content

<p>1. Nanometer chip design overview</p>	<p>Learning time: 25h Theory classes: 3h Laboratory classes: 6h Self study : 16h</p>
<p>Description:</p> <ul style="list-style-type: none"> - Challenges in nanometer chip design - Digital design flows - Design and verification - Physical implementation - Low power design techniques - Test techniques - Signoff - Lab1 	
<p>2. RTL synthesis for low power</p>	<p>Learning time: 25h Theory classes: 3h Laboratory classes: 4h Self study : 18h</p>
<p>Description:</p> <ul style="list-style-type: none"> - Power problem - Low power techniques - Power-aware synthesis (Lab2) 	
<p>3. Design planning/floorplanning</p>	<p>Learning time: 24h Theory classes: 2h Laboratory classes: 4h Self study : 18h</p>
<p>Description:</p> <ul style="list-style-type: none"> - Low power design flow - Floorplan - Power distribution plan - Lab3 	

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4. Physical design	Learning time: 27h Theory classes: 3h Laboratory classes: 6h Self study : 18h
Description: - Placement and optimization - Clock tree synthesis - Routing - Lab4	
5. Sign-off	Learning time: 6h Theory classes: 2h Self study : 4h
Description: - IR drop analysis - Design finishing and layout verification - Tapeout - Lab: project	
6. Design project	Learning time: 18h Laboratory classes: 6h Self study : 12h
Description: Implement an IP using low power flow.	

Qualification system

Continuous evaluation (CE):
 Partial exams: 25%
 Individual assessments: 25%
 Laboratory experiences: 50%

Final score: maximum (CE, Final exam)

Regulations for carrying out activities

Final exam: individual
 Individual works: Individual
 Research presentation: groups of two students
 Laboratory: groups of two students



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Bibliography

Complementary:

Wang, L.T.; Chang, Y.W.; Ting, K. (eds.). Electronic design automation: synthesis, verification, and test. Burlington, MA: Morgan Kaufmann Publishers/Elsevier, 2009. ISBN 9780123743640.

Others resources:

Slides of the course