270018 - AC - Computer Architecture

Coordinating unit: 270 - FIB - Barcelona School of Informatics
Teaching unit: 701 - AC - Department of Computer Architecture
Academic year: 2017
Degree: BACHELOR’S DEGREE IN INFORMATICS ENGINEERING (Syllabus 2010). (Teaching unit Compulsory) BACHELOR’S DEGREE IN ENGINEERING PHYSICS (Syllabus 2011). (Teaching unit Optional)
ECTS credits: 6 Teaching languages: Catalan, Spanish

Teaching staff

Coordinator: Josep Llosa Espuny (josepll@ac.upc.edu)
Others: Angel Olivé Duran (angel@ac.upc.edu)
Antonio Juan Hormigo (antonioj@ac.upc.edu)
Carles Hernandez Luz (carles.hernandez@bsc.es)
Carlos Alvarez Martinez (calvarez@ac.upc.edu)
Fermin Sánchez Carracedo (fermin@ac.upc.edu)
Miquel Moretó Planas (mmoreto@ac.upc.edu)
Teresa Monreal Arnal (teresa@ac.upc.edu)

Prior skills

Students are expected to have an understanding of statistics and probability, operating systems, digital circuits and computer organization.

Requirements

- Prerequisite SO
- Pre-Corequisite PE
- Prerequisite EC

Degree competences to which the subject contributes

Specific:
CT2.3. To design, develop, select and evaluate computer applications, systems and services and, at the same time, ensure its reliability, security and quality in function of ethical principles and the current legislation and normative.
CT2.4. To demonstrate knowledge and capacity to apply the needed tools for storage, processing and access to the information system, even if they are web-based systems.
CT3.6. To demonstrate knowledge about the ethical dimension of the company: in general, the social and corporative responsibility and, concretely, the civil and professional responsibilities of the informatics engineer.
CT5.2. To know, design and use efficiently the most adequate data types and data structures to solve a problem.
CT6.2. To demonstrate knowledge, comprehension and capacity to evaluate the structure and architecture of computers, and the basic components that compound them.
CT7.1. To demonstrate knowledge about metrics of quality and be able to use them.
CT7.2. To evaluate hardware/software systems in function of a determined criteria of quality.
CT7.3. To determine the factors that affect negatively the security and reliability of a hardware/software system, and minimize its effects.
CT8.1. To identify current and emerging technologies and evaluate if they are applicable, to satisfy the users needs.
Learning objectives of the subject

1. Students should be able to translate routines and high-level code fragments to assembly of a real machine (IA32) and link routines in assembler with a high-level language (C) using the Linux Application Binary Interface.
2. Students should be able to describe the internal structure and operation of the main components of the memory hierarchy and the techniques to improve their performance.
3. Students should be able to describe the operation and to use the main mechanisms for error detection and correction.
4. Students should be able to describe the structure and operation of data storage systems and evaluate their reliability.
5. Students should be able to describe the taxonomy of instruction sets (ISA) and the characteristics of the different paradigms (such as RISC-CISC).
6. Students should be able to describe the techniques used in computer design based on parallelism (such as pipelining, superscalar processors, VLIW processors, vector SIMD extensions, multithreading processors, multiprocessors and multicomputers) and their principles of operation.
7. Students should be able to evaluate the performance of code fragments and/or applications (both in assembler and high level) taking into account components such as: memory hierarchy, storage systems, instruction set architecture (ISA) and the main processor design techniques based on parallelism.
8. Students should be able to assess the impact on power and energy consumption of code fragments and/or applications (in both assembler and high level) taking into account components such as: memory hierarchy, storage systems, the design of the instruction set architecture (ISA) and the main processor design techniques based on parallelism.
9. Students should be able to apply simple optimizations to code fragments to improve their performance and/or power consumption taking into account: the memory hierarchy, storage systems, the design of the instruction set architecture (ISA) and the main processor design techniques based on parallelism.

Teaching methodology

Theory lectures interleaved with small problems. In the theory classes homework will be assigned to students for the next practice class.

Problem-solving classes are based on group activities. Using problems solved individually at home, students will work together in small groups to resolve the doubts that may have emerged. Because the methodology used in practice classes it is recommended that students do not enroll to courses that overlap with this one.

The laboratory classes support the theory. Students have the documentation available before each practice session. It is mandatory that students prepare the session beforehand (read the documentation, study the concepts used, etc.). It is also recommended, once the session ends, to review the concepts seen. Students have to prepare a preliminary work that will be delivered at the beginning of each session. The lab sessions are performed on-site and used to produce the lab grade, so it is essential that there is no overlap of the laboratory with any other course.

Generical:

G2. SUSTAINABILITY AND SOCIAL COMPROMISE: to know and understand the complexity of the economic and social phenomena typical of the welfare society. To be capable of analyse and evaluate the social and environmental impact.
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## Study load

<table>
<thead>
<tr>
<th>Total learning time: 150h</th>
<th>Hours large group: 30h</th>
<th>20.00%</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Hours medium group: 15h</td>
<td>10.00%</td>
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<tr>
<td></td>
<td>Hours small group: 15h</td>
<td>10.00%</td>
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<tr>
<td></td>
<td>Guided activities: 6h</td>
<td>4.00%</td>
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<tr>
<td></td>
<td>Self study: 84h</td>
<td>56.00%</td>
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</tbody>
</table>

## Content

### Fundamentals of computer design and evaluation

Degree competences to which the content contributes:

### High-level / assembler language interface

Degree competences to which the content contributes:

### Memory Hierarchy

Degree competences to which the content contributes:

### Storage Systems

Degree competences to which the content contributes:

### Instruction Set Architecture Design

Degree competences to which the content contributes:

### Pipelining and parallelism in computer design

Degree competences to which the content contributes:
# Planning of activities

| C1 | Specific objectives: 1, 7, 8, 9 | Hours: 4h 30m  
Guided activities: 1h 30m  
Self study: 3h |
| --- | --- | --- |
| Fundamentals of computer design and evaluation | Specific objectives: 7, 8 | Hours: 10h  
Theory classes: 2h  
Practical classes: 1h  
Laboratory classes: 1h  
Guided activities: 0h  
Self study: 6h |
| C2 | Specific objectives: 1, 2, 7, 8, 9 | Hours: 5h  
Guided activities: 2h  
Self study: 3h |
| High-level/assembly language interface | Specific objectives: 1, 7, 8, 9 | Hours: 32h  
Theory classes: 4h  
Practical classes: 3h  
Laboratory classes: 5h  
Guided activities: 0h  
Self study: 20h |
| C3 | Specific objectives: 1, 2, 3, 4, 5, 6, 7, 8, 9 | Hours: 7h  
Guided activities: 3h  
Self study: 4h |
<table>
<thead>
<tr>
<th>Course Topic</th>
<th>Hours</th>
<th>Specific Objectives</th>
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</thead>
<tbody>
<tr>
<td>Memory Hierarchy</td>
<td>47h</td>
<td>2, 3, 7, 8, 9</td>
</tr>
<tr>
<td>Storage Systems</td>
<td>17h</td>
<td>3, 4, 7, 8, 9</td>
</tr>
<tr>
<td>Instruction set design</td>
<td>10h</td>
<td>5, 7, 8, 9</td>
</tr>
<tr>
<td>Pipelining and parallelism in computer design</td>
<td>14h</td>
<td>6, 7, 8, 9</td>
</tr>
<tr>
<td>Theory classes:</td>
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<td>Practical classes:</td>
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<td>Laboratory classes:</td>
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<tr>
<td>Guided activities:</td>
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<tr>
<td>Self study:</td>
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**Hours**: 47h

**Theory classes**: 10h

**Practical classes**: 5h

**Laboratory classes**: 4h

**Guided activities**: 0h

**Self study**: 28h
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**Visita Supercomputador Marenostrum**

<table>
<thead>
<tr>
<th>Hours:</th>
<th>2h</th>
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<tbody>
<tr>
<td>Theory classes:</td>
<td>2h</td>
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<tr>
<td>Practical classes:</td>
<td>0h</td>
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<tr>
<td>Laboratory classes:</td>
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<tr>
<td>Guided activities:</td>
<td>0h</td>
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<tr>
<td>Self study:</td>
<td>0h</td>
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**Specific objectives:**
2, 3, 4, 5, 6

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**Qualification system**

The grade for the course is calculated from 2 grades: Theory (80%) and laboratory (20%).

The laboratory grade (Lab) is obtained from the grades of the lab sessions.

During the course there are three controls C1, C2 and C3 with weights 1/6, 1/3 and 1/2 respectively. The theory grade (T) is calculated as the weighted arithmetic mean of the 3 controls.

\[ T = \frac{1}{6} \times C1 + \frac{1}{3} \times C2 + \frac{1}{2} \times C3 \]

The student final grade through continuous assessment (AC) will be:

\[ \text{Grade} = 0.2 \times \text{L} + 0.8 \times T \]

There is no final exam.

**Bibliography**

**Basic:**


**Complementary:**
