270060 - AC2 - Computer Architecture II

Coordinating unit: 270 - FIB - Barcelona School of Informatics
Teaching unit: 701 - AC - Department of Computer Architecture
Academic year: 2017
Degree: BACHELOR'S DEGREE IN INFORMATICS ENGINEERING (Syllabus 2010). (Teaching unit Optional)
ECTS credits: 6
Teaching languages: Catalan, Spanish

Teaching staff

Coordinator: - Angel Olivé Duran (angel@ac.upc.edu)

Prior skills


Requirements

- Prerequisite AC

Degree competences to which the subject contributes

Specific:
CEC1.1. To design a system based on microprocessor/microcontroller.
CEC1.2. To design/configure an integrated circuit using the adequate software tools.
CEC2.1. To analyse, evaluate, select and configure hardware platforms for the development and execution of computer applications and services.
CEC3.2. To develop specific processors and embedded systems; to develop and optimize the software of these systems.
CT6.2. To demonstrate knowledge, comprehension and capacity to evaluate the structure and architecture of computers, and the basic components that compound them.
CT7.1. To demonstrate knowledge about metrics of quality and be able to use them.

General:
G9. PROPER THINKING HABITS: capacity of critical, logical and mathematical reasoning. Capacity to solve problems in her study area. Abstraction capacity: capacity to create and use models that reflect real situations. Capacity to design and perform simple experiments and analyse and interpret its results. Analysis, synthesis and evaluation capacity.

Teaching methodology

In the theory classes expose the concepts of the course with student participation.
The exercise classes the students apply the theoretical concepts in solving exercises.
In laboratory classes students work in small groups and apply the concepts on a simple pipelined processor.

Learning objectives of the subject

1. Understanding concurrency techniques transparent to the programmer of machine language used by processors to reduce the execution time.
2. Understand some of the technological constraints in the implementation of a processor.
3. Knowledge of a hardware description language (VHDL) and application in the design of digital systems.
4. Training to assess the performance of a processor.
6. Basic understanding of the processor microarchitecture.

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<thead>
<tr>
<th>Study load</th>
<th>Hours large group:</th>
<th>30h</th>
<th>20.00%</th>
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<tbody>
<tr>
<td></td>
<td>Hours medium group:</td>
<td>15h</td>
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<td>Hours small group:</td>
<td>15h</td>
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<td></td>
<td>Guided activities:</td>
<td>6h</td>
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<td></td>
<td>Self study:</td>
<td>84h</td>
<td>56.00%</td>
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### Content

<table>
<thead>
<tr>
<th>Section</th>
<th>Degree competences to which the content contributes</th>
<th>Description</th>
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</thead>
</table>
| **Von-Neumann architecture and performance.**                          |                                                      | **Degree competences to which the content contributes:** 
Von-Neumann machine. Performance metrics. Manufacturing Technology. **Description:** |
| **Techniques to increase the number of operations per unit time.**     |                                                      | **Degree competences to which the content contributes:** 
Pipelining and replication. Interpretation of instructions. Structural hazards. **Description:** |
| **Linear pipeline processor.**                                         |                                                      | **Degree competences to which the content contributes:** 
Datapath. Dependencies between instructions. Data hazards. Control hazards. **Description:** |
| **Techniques to reduce and tolerate the pipeline effective latency.**  |                                                      | **Degree competences to which the content contributes:** 
Static instruction scheduling. Data bypasses. Fixed branch prediction. **Description:** |
| **Pipeline with multicycle operations.**                               |                                                      | **Degree competences to which the content contributes:** 
Multicycle operations. Datapath with parallel pipelines. Code transformations to exploit instruction-level parallelism. **Description:** |
# 270060 - AC2 - Computer Architecture II

## Planning of activities

<table>
<thead>
<tr>
<th>Topic</th>
<th>Hours</th>
<th>Theory classes</th>
<th>Practical classes</th>
<th>Laboratory classes</th>
<th>Guided activities</th>
<th>Self study</th>
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<tbody>
<tr>
<td><strong>Design tools and simulation</strong></td>
<td>15h</td>
<td>0h</td>
<td>0h</td>
<td>6h</td>
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<td>9h</td>
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<tr>
<td>Learning tools for specification and simulation of logic circuits.</td>
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<td>Review of the operation and basic characteristics of the components</td>
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<td>of a single-cycle datapath.</td>
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<tr>
<td><strong>Von-Neumann machine and performance</strong></td>
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<td>2h</td>
<td>0h</td>
<td>0h</td>
<td>10h</td>
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<td>Development of item 1 of the course</td>
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<td><strong>Techniques to increase the number of operations per unit time</strong></td>
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<td>5h</td>
<td>3h</td>
<td>0h</td>
<td>0h</td>
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<td>1, 4, 6</td>
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<tr>
<td><strong>Linear pipeline processor</strong></td>
<td>28h</td>
<td>7h</td>
<td>3h</td>
<td>4h</td>
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<td>14h</td>
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<td><strong>Specific objectives:</strong></td>
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## Description:
Development of item 3 of the course

**Specific objectives:**
1, 4, 6

### Partial Test

**Hours:** 10h
- Guided activities: 2h
- Self study: 8h

**Specific objectives:**
1, 2, 4, 6

### Techniques to reduce and tolerate pipeline effective latency

**Hours:** 30h
- Theory classes: 7h
- Practical classes: 4h
- Laboratory classes: 5h
- Guided activities: 0h
- Self study: 14h

**Description:**
Development of item 4 of the course

**Specific objectives:**
1, 4, 6

### Processor with multicycle operations

**Hours:** 19h
- Theory classes: 5h
- Practical classes: 3h
- Laboratory classes: 0h
- Guided activities: 0h
- Self study: 11h

**Description:**
Development of item 5 of the course

**Specific objectives:**
1, 4, 6

### Consolidation

**Hours:** 3h
- Theory classes: 0h
- Practical classes: 0h
- Laboratory classes: 0h
- Guided activities: 3h
- Self study: 0h
Final Exam

**Hours:** 11h
- Guided activities: 3h
- Self study: 8h

**Specific objectives:**
1, 2, 3, 4, 6

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**Qualification system**

There are three elements:

Final (F): final written exam covering all the objectives of the course. Partial (P): written test on the first three topics. Lab (L) from the reports made in each of the sessions and, where appropriate, a personal interview.

\[ NF = 0.2 \times L + \max(0.8 \times F, (0.65 \times F + 0.15 \times P)) \]

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**Bibliography**

**Basic:**


**Complementary:**