Course guide
330109 - SD - Digital Systems

Last modified: 24/05/2026

Unit in charge: Manresa School of Engineering
Teaching unit: 750 - EMIT - Department of Mining, Industrial and ICT Engineering.

Degree: BACHELOR'S DEGREE IN INDUSTRIAL ELECTRONICS AND AUTOMATIC CONTROL ENGINEERING (Syllabus 2016). (Compulsory subject).
BACHELOR'S DEGREE IN AUTOMOTIVE ENGINEERING (Syllabus 2017). (Optional subject).

Academic year: 2026 **ECTS Credits:** 6.0 **Languages:** Catalan, English

LECTURER

Coordinating lecturer: Comerma Montells, Albert

Others:

REQUIREMENTS

Have approved or taken Digital Electronics (330105).

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
1. (ENG) L'assignatura contribueix a desenvolupar:
- La capacitat d'especificar, analitzar, dissenyar, avaluar i documentar circuits digitals, tant seqüencials com combinacionals, així com les seves alternatives d'implementació, incloent dispositius CPLD i FPGA.
- La capacitat d'emprar les eines i els llenguatges d'especificació, síntesi i verificació de circuits digitals.
- El coneixement i la capacitat d'emprar les eines i la instrumentació existents per a l'anàlisi, el disseny, el desenvolupament i la verificació de sistemes electrònics, informàtics i de comunicacions.
2. The ability to use the tools and languages of specification, synthesis and verification of electronic circuits.
3. The knowledge and ability to use existing tools and instrumentation for the analysis, design, development and verification of electronic, computer and communications systems.

Transversal:
4. THIRD LANGUAGE. Learning a third language, preferably English, to a degree of oral and written fluency that fits in with the future needs of the graduates of each course.
5. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 3. Communicating clearly and efficiently in oral and written presentations. Adapting to audiences and communication aims by using suitable strategies and means.
6. SELF-DIRECTED LEARNING - Level 3. Applying the knowledge gained in completing a task according to its relevance and importance. Deciding how to carry out a task, the amount of time to be devoted to it and the most suitable information sources.

TEACHING METHODOLOGY

The subject consists of face-to-face activities consisting of 3 hours per week of class and 2 hours per fortnight of laboratory practices. The student carries out learning through various mechanisms. In the lectures and participative classes the contents of the subject are presented and the interaction between students and teacher is facilitated. Individual / group personal work activities are also proposed that should contribute to the understanding of the subject.
In laboratory classes, students may carry out preliminary work that helps to put into context the work that is intended to be carried out in the laboratory. The laboratory activity itself is developed in groups of two students and allows experimenting with certain aspects of the subject. The writing of the memory and the interaction with the teacher in the laboratory allows working on the oral and written communication skills and the third language knowledge and evaluation.
The use of generative AI is permitted in this course, but it must be done reasonably and must be specified in any deliverable where and how it has been used.

LEARNING OBJECTIVES OF THE SUBJECT

Upon completion of the student student's Digital Systems course:

- You will know the fundamentals of programmable devices (CPLD, FPGA) and will be able to analyze, design and implement digital circuits of general scope and medium complexity.
- You will be able to write simple technical reports and present them orally.

STUDY LOAD

Type	Hours	Percentage
Hours small group	15,0	10.00
Self study	90,0	60.00
Hours large group	45,0	30.00

Total learning time: 150 h

CONTENTS

1. INTRODUCTION TO PROGRAMMABLE DEVICES

Description:
This topic presents the alternatives of digital design and the area where programmable devices (CPLD and FPGA) will be the best design option. It also points out about the different methods to describe digital hardware. The vehicular method of the subject will be VHDL.

Related activities:
All.

Full-or-part-time: 11h
Theory classes: 3h
Practical classes: 2h
Self study : 6h

2. PROGRAMMABLE DEVICES

Description:
In this topic it is intended that the student can:
- Know and remember the main programmable digital elements and recognize the different architectures and characteristics of a device by reading its specification sheets.
- Know how to find the best design option (speed, consumption, ...) searching between manufacturers and components.
- Know the peculiarities of a real assembly based on a CPLD / FPGA and know how to apply them.

Related activities:
All.

Full-or-part-time: 16h
Theory classes: 4h
Practical classes: 4h
Self study : 8h

3. DEVICE-BASED DIGITAL DESIGN

Description:
In this topic it is intended that the student can:
- Know and remember the main digital basic blocks and their definition in VHDL.
- Know how to design digital systems of moderate complexity and know how to create the necessary stimuli to verify their proper functioning.
- Know how to study simple protocols of commercial devices and implement the digital hardware necessary to communicate with these devices.
- Know the basic modules that make up a simple computer and how an assembly instruction execution is produced.

Related activities:
All

Full-or-part-time: 123h
Theory classes: 38h
Practical classes: 9h
Self study : 76h

ACTIVITIES

TITLE OF ACTIVITY 1: MASTER AND PARTICIPATORY CLASSES

Description:
In the classes the theoretical aspects of the subject will be developed. These will allow interaction between the students and the teacher.

Specific objectives:
- Know how to design digital circuits described in VHDL and recognize the basic digital blocks associated with this VHDL description.
- Know how to design the stimuli that allow to verify a digital circuit.
- Understand the specification sheets of commercial programmable devices.
- Understand a simple real protocol and know how to implement it with digital hardware.
- Know and know what it takes to put a programmable device (CPLD, FPGA) into practice.

Material:
Published teaching material.
Recommended bibliography.

Delivery:
Occasionally some evaluable activity will be carried out, which will contribute in a proportional part to the EXE variable.

Full-or-part-time: 40h
Theory classes: 40h

TITLE OF ACTIVITY 2: LABORATORY CLASSES

Description:
The practices to be carried out in the laboratory will be two hours a fortnight, in groups of two people. The student will have the statement of the practice that must be uploaded to the Athena. The laboratory will have a computer equipped with the necessary software to simulate digital components. Likewise, the necessary hardware will be available to experiment on commercial digital devices. The teacher will monitor the evolution of the students in particular. At the end of each practice, each group will send an email to the practice teacher attaching a file where the work done and the knowledge acquired will be explained.

Specific objectives:
- Implement the laboratory digital circuits based on FPGA and VHDL.
- Validate the operation of both simulated and physical digital circuits.
- Write and present documents reflecting the design and validation process of digital circuits.

Material:
Electronic equipment, breadboard, digital devices, computer with suitable software. Development board based on FPGA.
Statement of the practice and supporting information to carry out the work.

Delivery:
Before carrying out the practice, the students will deliver the previous individual study corresponding to the practice to be carried out.
During the session, the achievement of the objectives of each laboratory session will be assessed, taking into account the degree of understanding of the work demonstrated by each student.
At the end of the session, each working group will prepare a final report that reflects the main features of the actual work.
The qualification obtained in these activities configures the LAB variable.

Full-or-part-time: 25h
Laboratory classes: 15h
Self study: 10h

TITLE OF ACTIVITY 3: INDIVIDUAL / GROUP PERSONAL WORK

Description:
The student must develop certain activities personally to achieve the objectives of the subject.

Specific objectives:
All of the subject.

Material:
Published teaching material.
Recommended bibliography.

Delivery:
Individual / group personal work will be translated, in part, into exercises during the course. The grading of these exercises will contribute to the EXE variable.

Full-or-part-time: 50h
Self study: 50h

TITLE OF ACTIVITY 4: TESTS

Description:
During the course there will be an individual control test. At the end of the course there will be a final globalizing test of the knowledge acquired.

Material:
Test statements.

Delivery:
The control test score sets the variable CON.
The final test grade sets the FIN variable.

Full-or-part-time: 35h
Theory classes: 5h
Self study: 30h

GRADING SYSTEM

Any academic fraud, plagiarism or use or possession of unauthorised means in an assessment activity leads to a mark of zero (0) for the affected test or assignment. Furthermore, in accordance with the University's regulations, if disciplinary proceedings are initiated the subject is recorded as "Pending Assessment" until a decision is reached. These incidents are managed in accordance with the **Action Framework for Academic Integrity in Assessment at the UPC**.

The final grade for the course will be obtained as follows, EXE (exercises), CON (mid term exams), LAB (Laboratory), END (Final exam);
Final grade = MAX(0.15*CON+0.35*END, 0.5*END) + 0.1*EXE + 0.4*LAB
For the individual evaluation exams MAX(0.15*CON+0.35*END, 0.5*END) a minimum weighted average of 3.5 must be obtained to add the rest of grades; if this grade is not achieved the final grade will be equal to this individual evaluation exams weighted average; MAX(0.3*CON+0.7*END, END).
For the exercises, several activities will be proposed during the course at class or using the virtual campus platform.
The laboratory sessions will be evaluated using a FINAL TEST and with the activities carried out during the sessions. For each lab session a report must be delivered that may be evaluated, but will be the basis for study for the final control. During the laboratory sessions presence control may be performed; failing to attend at least 80% of the sessions without justification will automatically mean not to pass this part of the course.

EXAMINATION RULES.

In the case of laboratory activities for which a previous study has been established, it will be mandatory to submit it before accessing the laboratory.
Those activities that are explicitly declared as individual, whether in person or not, will be carried out without any collaboration from other people.
The dates, formats and other delivery conditions that are established will be mandatory.

BIBLIOGRAPHY

Basic:
- Ashenden, Peter J. Digital design: an embedded systems approach using VHDL [on line]. Burlington: Morgan Kaufmann, 2007 [Consultation: 31/05/2022]. Available on: https://ebookcentral-proquest-com.recursos.biblioteca.upc.edu/lib/upcatalunya-ebooks/detail.action?docID=858615. ISBN 9780123695284.
- Katz, R. H.; Borriello, G. Contemporary logic design. 2nd ed. Upper Saddle River: Pearson, 2005. ISBN 0131278304.