Course guide
230019 - DGD - Digital Design

Last modified: 11/04/2025

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: BACHELOR'S DEGREE IN TELECOMMUNICATIONS TECHNOLOGIES AND SERVICES ENGINEERING (Syllabus 2015). (Compulsory subject).
BACHELOR'S DEGREE IN DATA SCIENCE AND ENGINEERING (Syllabus 2017). (Optional subject).

Academic year: 2025 **ECTS Credits:** 6.0 **Languages:** Catalan

LECTURER

Coordinating lecturer: DIEGO CESAR MATEO PEÑA

Others: Primer quadrimestre:
JOSEP ALTET SANAHUJES - 11, 12, 13
DANIEL BARDES LLORENSI - 11, 13, 41, 42, 43
KRISTEL MICHELLE CEDEÑO MATA - 23, 42
JORDI COSP VILELLA - 12
PAU ESTARLICH GIL - 21
ROMÀ MACARIO CHIB - 43
DIEGO CESAR MATEO PEÑA - 21, 23
GERARD RIVERA VILA - 41

PRIOR SKILLS

Basic analysis of electronic circuits.
Basic knowledge of electronic devices and, in particular, the MOS transistor.

REQUIREMENTS

FONAMENTS D'ELECTRÒNICA - Precorequisit

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Generical:
12 CPE N2. They will be able to identify, formulate and solve engineering problems in the ICC field and will know how to develop a method for analysing and solving problems that is systematic, critical and creative.

TEACHING METHODOLOGY

Lectures and application classes
Laboratory classes
Group work (distance)
Individual work (distance)
Exercises
Short answer tests (Control)
Long answer tests (Final Exam)
Laboratory work

LEARNING OBJECTIVES OF THE SUBJECT

The student must be able to analyze, design and experimentally verify combinational and sequential digital subsystems. This course introduces and uses the hardware description language VHDL. It also includes an introduction to CMOS logic circuits, an introduction and utilización of programmable logic devices and an introduction to complex digital systems.

STUDY LOAD

Type	Hours	Percentage
Hours large group	39,0	26.00
Hours small group	26,0	17.33
Self study	85,0	56.67

Total learning time: 150 h

CONTENTS

Module 1. Introduction to digital design

Description:
The digital abstraction, systems and digital signals, behavior vs. structure, hierarchical design. Logic functions and Boolean algebra. Number systems and codes. Under the digital abstraction: power, delay, power consumption, logic levels and high impedance.

Full-or-part-time: 8h
Theory classes: 3h
Self study : 5h

Module 2. Combinational design

Description:
SdP and PdS canonic design. Combinational design based on logic gates and on standard combinational modules. Multiplexers, decoders, adders, comparators, etc.

Full-or-part-time: 36h
Theory classes: 6h
Laboratory classes: 6h
Self study : 24h

Module 3. Combinational design with VHDL

Description:
History and basic features of HDLs, methodologies and design tools. Basic elements: data types, objects, operators. Units Description: entities, architectures, packages and libraries. Concurrent assignments, conditional assignments and selections. Processes and sequential statements. Declaration and instantiation of components.

Full-or-part-time: 26h
Theory classes: 6h
Laboratory classes: 6h
Self study : 14h

Module 4. Sequential design

Description:
Asynchronous and synchronous sequential systems, time behavior. Latches and flip-flops. Analysis and synthesis of synchronous state machines. Sequential modular design, registers and counters. Sequential design with VHDL. Time performance: output delay, hold time, setup time, skews, maximum frequencies,clock and reset signal managing. Algorithmic machines, data unit and control unit.

Full-or-part-time: 59h
Theory classes: 13h 30m
Laboratory classes: 12h
Self study : 33h 30m

Module 5. CMOS digital circuits

Description:
Types of digital ICs and logic families. MOS transistors. CMOS inverter and basic logic gates. CMOS features: circuit delays, spurious, static and dynamic power consumption. Programmable logic devices, logic cells, and types of synthesis.

Full-or-part-time: 20h
Theory classes: 7h 30m
Self study : 12h 30m

GRADING SYSTEM

Final grade based on the respective qualifications of the theory (60%) and the laboratory (40%) parts. The theory mark consists of 70% from the final theory exam and 30% from the control at the midle of the term and the delivery of activities done during the course. If the grade corresponding to the previous 30% is smaller than that of the final theory exam, this one becomes the 100% of the theory grade.The laboratory mark is obtained from the laboratory work done during the course and from the final lab exam.

The re-evaluation of the course involves having to do the final exam again, which includes theory and laboratory parts. Grades earned replace the previous ones. Laboratory work together with control and/or delivered activities are not re-avaluable.

EXAMINATION RULES.

During the exams it is not allowed to use wireless devices (mobile phones, laptops, tablets, etc..) nor programmable calculators. It is also necessary to provide some identification document (ID card, passport, etc.)

BIBLIOGRAPHY

Basic:
- Harris, S.L; Money, D. Digital design and computer architecture. Waltham, MA: Morgan Kaufmann, 2016. ISBN 9780128000564.
- Pardo Carpio, F.; Boluda Grau, J.A. VHDL: lenguaje para síntesis y modelado de circuitos. 3a ed. act. Madrid: Ra-ma, 2011. ISBN 9788499640402.
- Ercegovac, M.D.; Lang, T.; Moreno, J.H. Introduction to digital systems. Estats Units d'Amèrica: John Wiley & Sons, 1999. ISBN 0471527998.

RESOURCES

Computer material:
- Quartus II Web edition