Course guide
230652 - ESDC - Electronic System Design for Communications

Last modified: 11/04/2025

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: MASTER'S DEGREE IN TELECOMMUNICATIONS ENGINEERING (Syllabus 2013). (Compulsory subject).
MASTER'S DEGREE IN ADVANCED TELECOMMUNICATION TECHNOLOGIES (Syllabus 2019). (Optional subject).

Academic year: 2025 **ECTS Credits:** 5.0 **Languages:** English

LECTURER

Coordinating lecturer: JOSEP ALTET SANAHUJES

Others: Primer quadrimestre:
JOSEP ALTET SANAHUJES - 11, 13
FRANCESC DE BORJA MOLL ECHETO - 11, 13

PRIOR SKILLS

Previous knowledge needed to follow all the explanations:
BASIC CIRCUIT ANALYSIS:
- RC circuits. Time constant. Energy stored in a capacitor.
MOS TRANSISTOR
- Identification of terminals, currents and voltages in NMOS and PMOS devices.
- Large Signal (DC), long channel equations (ID vs VGS, VDS) curves and regions. Transconductance and gate dimensions. Channel-Length modulation. Overdrive voltage
- Unified model for PMOS and NMOS.
- Threshold voltage effects: Body Effect. Threshold voltage as a function of bulksource voltage: linear simplification equation. Drain induced barrier lowering.
- Short channel equations: Mobility degradation and Velocity saturation.
- Parasitic capacitances: Gate capacitance and Diffusion Capacitance
DIGITAL CIRCUITS
- CMOS Logic gates. Extraction of the truth table and logic expression from a gate transistor schematic.
DIGITAL DESIGN
- Digital codes: Signed and unsigned binary codes. Basic binary arithmetic operations: addition and multiplication. Error Detection Codes: parity codes.
- Combinational circuits. Canonical implementation of logic functions. De Morgan's Laws.
- State Machines: state diagram. Canonical structure of sequential systems.
- Basic combinational and seqüential blocks. Truth table. Logic level schematic. Symbol. (basic logic gates, multiplexer, decoder, half adder, full adder, flip-flop, latch, register, counter).
- Digital waveform as a function of time interpretation.
- VHDL Hardware Description Language.

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
1. Ability to design and manufacture integrated circuits
2. Knowledge of hardware description languages for high-complex circuits.
3. Ability to use programmable logical devices, as well as to design analog and digital advanced electronics systems. Ability to design communication devices, such as routers, switches, hubs, transmitters and receivers in different bands.

Transversal:
4. EFFECTIVE USE OF INFORMATION RESOURCES: Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.

5. FOREIGN LANGUAGE: Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

TEACHING METHODOLOGY

- Lectures
- Learning by doing: design development.
- Individual and team work

LEARNING OBJECTIVES OF THE SUBJECT

Know the general principles and design methodologies of digital circuits dedicated to communication and processing.
Ability to design the main blocks of a digital electronic system with communications applications.
Estimate and calculate figures of merit in digital circuits related to timing and power consumption.

STUDY LOAD

Type	Hours	Percentage
Hours small group	13,0	10.40
Hours large group	26,0	20.80
Self study	86,0	68.80

Total learning time: 125 h

CONTENTS

T1. Introduction

Description:
Objectives for the course. General view of a communication system design. Implementation options. Design example overview.

Full-or-part-time: 2h
Theory classes: 1h
Self study : 1h

T2. Auxiliary blocks

Description:
Timer. Queue. simple UART.

Full-or-part-time: 17h
Theory classes: 5h
Self study : 12h

T3. Communication flow control

Description:
UART with Timeout.

Full-or-part-time: 18h
Theory classes: 6h
Self study : 12h

T4. Error checking and protocol implementation

Description:
CRC generator and checker. Integration with UART with Timeout.

Full-or-part-time: 18h
Theory classes: 6h
Self study : 12h

T5. Timing aspects in digital design

Description:
Delay modeling. Timing analysis.

Full-or-part-time: 14h
Theory classes: 4h
Self study : 10h

T6. Power consumption in digital design

Description:
Power consumption modeling. Low power techniques.

Full-or-part-time: 14h
Theory classes: 4h
Self study : 10h

L1: Timer

Description:
Timer design with Quartus software

Full-or-part-time: 9h
Laboratory classes: 3h
Self study : 6h

L2: Queues and CRC

Description:
Design of a queue and a CRC system.

Full-or-part-time: 7h
Laboratory classes: 2h
Self study : 5h

L3: TX-RX Timer

Description:
Design of an UART with Timeout.

Full-or-part-time: 7h
Laboratory classes: 2h
Self study : 5h

L4: TX-RX Timer CRC

Description:
Integration of CRC with UART and timeout.

Full-or-part-time: 7h
Laboratory classes: 2h
Self study : 5h

L5: TX-RX Timer CRC ACK

Description:
Protocol implementation for flow control.

Full-or-part-time: 6h
Laboratory classes: 2h
Self study : 4h

L6: Power analysis

Description:
Power analysis of the final implementation.

Full-or-part-time: 6h
Laboratory classes: 2h
Self study : 4h

GRADING SYSTEM

Final examination: 50%
Partial exams and laboratory: 50%.

BIBLIOGRAPHY

Basic:
- Franklin, M.A. [et al.]. Network Processor Design, vol. 3, Issues and practices [en línia] [on line]. Morgan Kaufmann, 2005 [Consultation: 21/04/2020]. Available on: https://ebookcentral.proquest.com/lib/upcatalunya-ebooks/detail.action?docID=232128. ISBN 9780120884766.
- Weste, N.H.E.; Harris, D.M. CMOS VLSI design: a circuits and systems perspective. 4th ed. Boston: Addison Wesley, 2011. ISBN 9780321547743.
- Forouzan, B. A. Data communications and networking with TCP/IP protocol suite. 6th ed. New York: McGraw-Hill, 2022. ISBN 9781260597820.
- Escudero i Costa, F; Altet, J. Design methodology for programming multi task applications on low cost microprocessors. First edition: English version. [Great Britain]: Francesc Escudero, Josep Altet, [2020]. ISBN 9798667923503.

Complementary:
- Giladi, R. Network Processors : architecture, programming, and implementation [on line]. Amsterdam: Morgan Kaufmann, 2008 [Consultation: 21/04/2020]. Available on: https://ebookcentral.proquest.com/lib/upcatalunya-ebooks/detail.action?docID=404833. ISBN 9780080919591.