Course guide
230731 - DND - Digital Nanoelectronic Design

Last modified: 11/04/2025

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: MASTER'S DEGREE IN TELECOMMUNICATIONS ENGINEERING (Syllabus 2013). (Optional subject).
MASTER'S DEGREE IN ADVANCED TELECOMMUNICATION TECHNOLOGIES (Syllabus 2019). (Optional subject).
MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2022). (Compulsory subject).

Academic year: 2025 **ECTS Credits:** 5.0 **Languages:** English

LECTURER

Coordinating lecturer: JORDI MADRENAS BOADAS - JORDI COSP VILELLA

Others: Primer quadrimestre:
JORDI MADRENAS BOADAS - 21, 23
FRANCESC DE BORJA MOLL ECHETO - 21, 23

PRIOR SKILLS

General concepts on microelectronic design.
- Characteristics of current technologies.
- Microelectronic technology, integrated circuit manufacturing.
- Design process (scheme) and physical description (layout) and verification.
- Behavior and basic equations of the MOS transistor.
- DC analysis of basic circuits.
- MOS transistor capacitance.
- CMOS digital gates speed and power consumption.

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
CMEE18. Design digital and analog CMOS integrated circuits of medium complexity.
CMEE19. Apply low-power techniques for integrated circuits (ICs).
CMEE20. Design for testability and develop test procedures for ICs.

Transversal:
CTMEE5. Third language. Know a third language, preferably English, with an adequate oral and written level and in line with the needs that graduates will have.

TEACHING METHODOLOGY

- Lectures
- Laboratory classes.
- Laboratory practical work.
- Short answer test (Control).
- Extended answer test (Final Exam).

LEARNING OBJECTIVES OF THE SUBJECT

The main learning result of the subject is:
- Ability to design digital medium-complexity CMOS integrated circuits, from hardware description to tapeout.
This is divided into the following specific objectives:
- Ability to understand the evolution of integrated technologies.
- Ability to identify cases and applications suitable for an integrated solution.
- Ability to analyze the characteristics of a digital integrated circuit.
- Ability to introduce low-power design techniques.
- Ability to evaluate the effect of interconnects and to consider them in the design.
- Ability to use ancillary elements, such as power and clock distribution, buffers, PLLs/DLLs, I/O pads and drivers.
- Ability to use industrial CAD/CAE tools for digital integrated design.

STUDY LOAD

Type	Hours	Percentage
Hours large group	26,0	20.80
Hours small group	13,0	10.40
Self study	86,0	68.80

Total learning time: 125 h

CONTENTS

1. Introduction

Description:
1.1 Moore's Law. CMOS limits and technology trends.
1.2 Cost performance tradeoff. Design space.
1.3 Planar MOSFET and FinFET models for digital design.
1.4 State of the art in VLSI.
1.5 SoC. Chip examples.

Full-or-part-time: 6h
Theory classes: 2h
Self study : 4h

2 Combinational circuit design

Description:
2.1 Structure of CMOS static gates.
2.2 Layout of CMOS static gates. Euler path method.
2.3 RC delay model. Elmore delay.
2.4 Logical effort. Propagation and contamination delay estimation.
2.5 Other circuit families: Ratioed, Dynamic, Pass-transistor, CVSL.

Full-or-part-time: 20h
Theory classes: 6h
Self study : 14h

3 Sequential CMOS circuit design

Description:
3.1 Latches and flip-flops. Setup and hold time.
3.2 Delay constraints. Clock skew.
3.3 Reset. D, E and T flip-flops.
3.4 Synchronizers. Timing analysis. Slack. Clock domain crossing.
3.5 Integrated memory: SRAM, DRAM, ROM and Flash.

Full-or-part-time: 14h
Theory classes: 4h
Self study : 10h

4 Digital subsystems

Description:
4.1 Structured design strategies. Hierarchy, Regularity, Modularity, Locality.
4.2 Control unit and datapath.
4.3 Counters, LFSRs and shifters. FIFO.
4.4 Binary adders.
4.5 Binary multipliers.

Full-or-part-time: 13h
Theory classes: 4h
Self study : 9h

5 Low-power design

Description:
5.1 Power dissipation sources. The importance of power consumption reduction.
5.2 Low-power design.
5.3 Dynamic power reduction. Clock gating. DVFS.
5.4 Static power reduction. Power gating. Multiple threshold
5.5 DVS.

Full-or-part-time: 7h
Theory classes: 2h
Self study : 5h

6 Practical aspects of VLSI design

Description:
6.1 Interconnect modeling. R, C, L. Skin effect.
6.2 Interconnect delay and energy.
6.3 Crosstalk.
6.4 Robustness and variability. Variability strategies. Design corners.
6.6 Power supply distribution.
6.7 Clock distribution. Buffering.
6.8 PLL and DLL.
6.9 Input/output pads.
6.10 Layout and tapeout: Floorplan, DRC, latchup, electromigration, parasitics, antenna effect.
6.11 Packaging.

Full-or-part-time: 13h
Theory classes: 4h
Self study : 9h

7 Test and verification

Description:
7.1 The need of manufacturing test. Defects and faults.
7.2 Fault models. Yield. Redundancy. Test vectors.
7.3 Fault coverage. Controllability and observability.
7.4 Automatic Test Pattern Generation (ATPG). Delay fault testing.
7.5 Design for test (DFT).
7.6 Scan-based test.
7.7 Built-In Self Test (BIST).
7.8 System-level test.
7.5 Design for test (DFT).
7.6 Scan-based test.
7.7 Fault tolerance and self test. BIST.
7.8 System-level test.

Full-or-part-time: 13h
Theory classes: 4h
Self study : 9h

Laboratory of digital VLSI design

Description:
Project design of a medium-complexity integrated circuit. CAE tools: synthesis and back-end. Layout design. Standard cell library. Functional and back-annotated simulation.

Full-or-part-time: 39h
Laboratory classes: 13h
Self study : 26h

GRADING SYSTEM

Final examination: 50%
Midterm examination: 20%
Laboratory assessments: 30%

BIBLIOGRAPHY

Basic:
- Weste, N.H.E.; Harris, D.M. CMOS VLSI design: a circuits and systems perspective. 4th ed. Boston: Addison Wesley, 2011. ISBN 9780321547743.

Complementary:
- Lin, Ming-Bo. Introduction to VLSI systems: a logic, circuit, and system perspective. Boca Ratón: CRC Press, 2012. ISBN 9781439868591.
- Rabaey, Jan. Low Power Design Essentials [on line]. New York, NY: Springer, 2009 [Consultation: 30/06/2022]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-0-387-71713-5. ISBN 9781282126534.
- Saha, Samar K. FinFET Devices for VLSI Circuits and Systems [on line]. Boca Raton, FL: CRC Press, 2021 [Consultation: 07/07/2022]. Available on: https://www.taylorfrancis.com/books/9780429504839. ISBN 9780429504839.