Course guide
230921 - SDC - Configurable Digital Systems

Last modified: 24/05/2024

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: BACHELOR'S DEGREE IN ELECTRONIC ENGINEERING AND TELECOMMUNICATION (Syllabus 2018). (Compulsory subject).

Academic year: 2024 **ECTS Credits:** 6.0 **Languages:** Catalan

LECTURER

Coordinating lecturer: JOAN PONS NIN

Others: Primer quadrimestre:
JUAN ANTONIO CHAVEZ DOMINGUEZ - 11, 12, 13
JOAN PONS NIN - 11, 12, 13

PRIOR SKILLS

Basic knowledge of CMOS technology.
Basic knowledge of combinational and sequential digital design.
Basic knowledge of microprocessor architectures.

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
CE15. (ENG) GREELEC: Coneixement i aplicació dels fonamentals llenguatges de descripció de dispositius de hardware. (Mòdul comú a la branca de telecomunicació).
CE24. (ENG) GREELEC: Capacitat per aplicar l'electrònica com tecnologia de suport a altres camps i activitats, i no només en l'àmbit de les tecnologies de la informació i comunicació. (Mòdul de tecnologia específica- Sistemes electrònics).
CE27. (ENG) GREELEC: Capacitat per a dissenyar dispositius d'interficíe, captura de dades i emmagatzament, i terminals per serveis i sistemes de telecomunicació. (Mòdul de tecnologia específica- Sistemes electrònics).

Transversal:
CT4. (ENG) GREELEC: TREBALL EN EQUIP: ser capaç de treballar com a membre d'un equip interdiscplinar, ja sigui com un membre més o realitzant tasques de direcció, amb la finalitat de contrinuir a desenvolupar projectes amb pragmatisme i sentit de la responsabillitat, assumint compromisos tenint en compte els recursos disponibles.

Basic:
CB4. (ENG) GREELEC: Que els estudiants poguin transmetre informació, idees, problemes i solucions a un públic tant esepecialitzat com no especialitzat.

TEACHING METHODOLOGY

Lectures: presentations on each specific topic and collective analysis of cases of electronic digital design.
Classes of problems: Study of digital design problems related to exposed theory.
Laboratory classes: Design, analysis and development of digital circuitry associated with the exposed theory and
realistic applications. These laboratory activities will be implemented in test & development boards based on programmable logic devices.
programmable devices.
Short-answer tests (controls) and extended-response (final exam)

LEARNING OBJECTIVES OF THE SUBJECT

The main objective will be the design of synchronous circuits of medium and high complexity for applications preferably communications and signal processing in real time.
Rapid prototyping is the focus of the subject. Implement efficient designs require good training in the hardware
description language VHDL, knowledge and use of design tools, architectures of FPGAs, as well as advanced digital design concepts.
The study and characterization of features, especially the temporal behavior of designs will also be important. Knowing the physical limitations of the devices is a priority to calculate the basic parameters of the circuits: maximum operating frequency, power dissipation, cost and occupied area.
Assimilation and consolidation of knowledge will be achieve implementing the designs in the laboratory with design tools and commercial devices.
List of specific objectives of the course:
* The use of methodologies and design tools for complex sequential digital systems.
* To analyze some of the issues of greatest impact in the digital design.
* Identify and evaluate alternative implementation of digital systems, including programmable logic devices.
* Understanding and using hardware description languages, including VHDL.

STUDY LOAD

Type	Hours	Percentage
Hours small group	26,0	17.33
Self study	85,0	56.67
Hours large group	39,0	26.00

Total learning time: 150 h

CONTENTS

Design of digital electronic systems

Description:
1.1. Design strategies.
1.2. Programmable logic devices: CPLDs, FPGAs.
1.3. Rapid prototyping tools.
1.3.1. Hardware description languages, types and levels of description.
1.3.2. Synthesis.
1.3.3. Simulation. Timing constraints and performance verification.
1.3.4. Guidelines for manufacturing test.

Full-or-part-time: 37h
Theory classes: 9h 45m
Laboratory classes: 6h 30m
Self study : 20h 45m

Synthesis with VHDL

Description:
2.1. Reminder of the main features.
2.2. Libraries.
2.3. Functions and procedures.
2.4. Inference of specific blocks.
2.4.1. Generation and distribution of clock signals.
2.4.2. Arithmetic blocks.
2.4.3. Memory blocks. Implementation of stacks.

Full-or-part-time: 37h
Theory classes: 9h 45m
Laboratory classes: 6h 30m
Self study : 20h 45m

Design techniques

Description:
3.1. Concurrent state machines.
3.2. Algorithmic machines.
3.2.1. Data subsystem. Pipelining.
3.2.2. Control subsystem.
3.2.3. Microprogrammable systems.
3.3. Methods to reduce consumption.
3.4. Structures and standards of test.
3.5. IP cores.

Full-or-part-time: 38h
Theory classes: 9h 45m
Laboratory classes: 6h 30m
Self study : 21h 45m

Design Issues

Description:
4.1. Timing of digital circuits.
4.1.1. Temporal analysis.
4.1.2. Metastability.
4.1.3. Hazards.
4.1.4. Synchronous versus asynchronous.
4.2. Synthesis of frequency.
4.3. Interface with memories and other peripherals.
4.4. Test.

Full-or-part-time: 38h
Theory classes: 9h 45m
Laboratory classes: 6h 30m
Self study : 21h 45m

GRADING SYSTEM

Continuous theory assessment: controls, exercises and / or works to be done during the course (CT)
Final theory exam (FTE)
Final theory grade of (FTG): Maximum (FTE , 0.5FTE + 0.5CT)
Continuous laboratory assessment (CL): Activity Tracking
Final Laboratory exam (FLE)
Final Laboratory grade (NLG): 0.75CL + 0.25 FLE
Final note subject = 0.5FTG + 0.5 NLG

The reassessment consists of taking the final theory (EFTR grade) and laboratory (EFLR grade) exams again.
Laboratory reassessment note (NRL): 0.75CL + 0.25 EFLR
Final reassessment grade = 0.5 EFTR + 0.5 NRL

EXAMINATION RULES.

Exams: Individual
Individual work: Individual
Laboratory groups: maximum two students.
The use of devices with a wireless connection (mobile phones, laptops, tablets, etc.) or programmable calculators is not allowed in the exams. In addition, it is necessary to have some identification document (DNI, NIE, passport, etc.)

BIBLIOGRAPHY

Basic:
- Gajski, D.D. Principles of digital design. Upper Saddle River, N.J.: Prentice Hall, 1997. ISBN 0132423979.
- Brown, S.; Vranesic, Z. Fundamentals of digital logic with VHDL design. 3rd ed. Boston: McGraw-Hill, 2009. ISBN 9780077221430.
- Skahill, K.; Legenhausen, J. VHDL for programmable logic. Reading: Addison-Wesley, 1996. ISBN 0201895730.
- Ashenden, P.J. The designer's guide to VHDL [on line]. 3rd ed. Burlington: Morgan Kaufmann, 2008 [Consultation: 15/07/2019]. Available on: https://www.sciencedirect.com/science/book/9780120887859. ISBN 9780120887859.