

Course guide

230930 - DMIC - Microelectronic Design

Last modified: 13/06/2024

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: BACHELOR'S DEGREE IN ELECTRONIC ENGINEERING AND TELECOMMUNICATION (Syllabus 2018).
(Compulsory subject).

Academic year: 2024 **ECTS Credits:** 6.0 **Languages:** Catalan, English

LECTURER

Coordinating lecturer: DIEGO CESAR MATEO PEÑA

Others: Primer quadrimestre:
XAVIER ARAGONES CERVERA - 11, 12, 13
ROGER FIGUERAS BAGUÉ - 12
DIEGO CESAR MATEO PEÑA - 11, 12, 13

PRIOR SKILLS

The MOS transistor - Physical structure and Modeling (DC equations). CMOS digital gates. Concepts of operation point (quiescent point) and response to the small signal. Small-signal model. DC and dynamic analysis of basic circuits. Circuit analysis in the Laplace domain.

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:

CE22. (ENG) GREELEC: Capacitat per a seleccionar circuits i dispositiu electrònics per a la transmissió, l'encaminament o enrutament i els terminals, tant en entorn fixs com mòbils. (Mòdul de tecnologia específica - Sistemes Electrònics).

CE27. (ENG) GREELEC: Capacitat per a dissenyar dispositius d'interfície, captura de dades i emmagatzament, i terminals per serveis i sistemes de telecomunicació. (Mòdul de tecnologia específica- Sistemes electrònics).

General:

CG4. (ENG) GREELEC: Capacitat de resoldre problemes amb iniciativa, presa de decisions, creativitat i de comunicació i transmetre coneixements, habilitats i destresa, comprnent la responsabilitat ètic i professional de l'activitat de l'enginyer tècnic de telecomunicació.

Transversal:

CT7. (ENG) GREELEC: TERCERA LENGUA: Conèixer una tercera llengua, preferentment l'anglès, amb un nivell adequat oral i escrit i en consonància amb les necessitats que obtindran els titulats i titulades.

CT4. (ENG) GREELEC: TREBALL EN EQUIP: ser capaç de treballar com a membre d'un equip interdisciplinar, ja sigui com un membre més o realitzant tasques de direcció, amb la finalitat de contrinuir a desenvolupar projectes amb pragmatisme i sentit de la responsabilitat, assumint compromisos tenint en compte els recursos disponibles.

Basic:

CB4. (ENG) GREELEC: Que els estudiants puguin transmetre informació, idees, problemes i solucions a un públic tant especialitzat com no especialitzat.

TEACHING METHODOLOGY

- Lectures
- Laboratory practical classes
- Individual work (distance)
- Group work (distance)
- Exercises
- Extended answer test (Mid-Term Exam)
- Extended answer test (Final Exam)

LEARNING OBJECTIVES OF THE SUBJECT

The main objective of this course is to provide the student with knowledge and fundamental capacities for the design of integrated circuits in CMOS microelectronic technologies. Starting from the analysis and design of both digital (gates) and analog (amplifier) basic circuits, the student will progress to the physical design of these circuits in CMOS integrated technologies (layout), and will know the processes of physical and functional verification of the designed circuits, which must be completed before being manufactured. The student will understand the physical aspects that affect the performance of the circuits (parasitic capacitances, process variability, noise), will know different non-idealities, and finally will be introduced in the specificities of the microelectronic design for radio frequency circuits.

STUDY LOAD

Type	Hours	Percentage
Self study	85,0	56.67
Hours small group	26,0	17.33
Hours large group	39,0	26.00

Total learning time: 150 h

CONTENTS

Integrated Cicuits Micro- and Nano-Electronic Technologies

Description:

General concepts on the past evolution of microelectronics and characteristics of the technologies today.
Microelectronic technology, manufacturing of integrated cicuits.

Full-or-part-time: 4h

Theory classes: 2h

Self study : 2h

Layout of a CMOS integrated cirucit

Description:

Step-by-step design process from the electrical circuit (schematics) to the physical description (layout) and verification. Use of CAD tools for the design of chips (Cadence Virtuoso IC design).

Related activities:

Labs

Full-or-part-time: 8h 50m

Theory classes: 1h

Laboratory classes: 2h

Self study : 5h 50m

MOS Transistor. DC circuit analysis (large signal)

Description:

Reminder: Behavior and basic equations for the MOS transistor.
DC analysis of basic circuits. Voltage-mode or current-mode biasing.

Related activities:

Labs

Full-or-part-time: 16h

Theory classes: 3h

Laboratory classes: 3h

Self study : 10h

Dynamic response of CMOS gates

Description:

Reminder: MOS transistor capacitances.
Speed in CMOS digital gates. Estimation of the propagation time.
Power consumption in CMOS digital gates (leakage and dynamic).
Buffer design.

Related activities:

Labs

Full-or-part-time: 34h

Theory classes: 9h

Laboratory classes: 6h

Self study : 19h

CMOS basic analog stages

Description:

Reminder: MOSFET small-signal model.
Common-source amplifier with load resistance
Current sources, current mirrors
Active loads.
Common-drain stage (source follower).
Frequency response in amplifiers.
Common-gate stage. Cascode structure.

Related activities:

Labs

Full-or-part-time: 32h

Theory classes: 9h

Laboratory classes: 4h

Self study : 19h

Differential stages

Description:

Basic definitions. Differential pair.
Differential pair with resistive load (fully-differential).
Differential pair with current mirror load (single-ended).

Related activities:

Labs.

Full-or-part-time: 17h 50m

Theory classes: 3h

Laboratory classes: 4h

Self study : 10h 50m

Degradation of the signal quality produced by noise and non-linearity

Description:

Noise
Non-linearity

Full-or-part-time: 16h 40m

Theory classes: 5h

Self study : 11h 40m

Amplifier circuits for high frequencies (RF)

Description:

Introduction to radio-communication front-ends.
Low-Noise Amplifiers in Receivers front-ends. Narrowband amplifiers.

Related activities:

Labs.

Full-or-part-time: 20h 40m

Theory classes: 4h

Laboratory classes: 5h

Self study : 11h 40m

GRADING SYSTEM

Labs (LAB): 40%

Continuous Assessment (AC): 20%

Final Exam (EX): 40%

The final grade (NF) is the highest of the following: $NF = 0,4*LAB + 0,2*AC + 0,4*EX$, or $NF = 0,4*LAB + 0,6*EX$

BIBLIOGRAPHY

Basic:

- Razavi, B. Fundamentals of microelectronics. Hoboken: John Wiley & Sons, 2008. ISBN 9780471478461.
- Weste, Neil H.E; Harris, David Money. CMOS VLSI design : a circuits and systems perspective. 4th ed. Boston: Addison Wesley, cop. 2011. ISBN 9780321547743.

Complementary:



- Carusone, T.C.; Johns, D.A.; Martin, K.W. Analog integrated circuit design. Int. stud. version. New York: John Wiley, 2013. ISBN 9781118092330.

RESOURCES

Other resources:

Course slides, exercises, and tutorials available through the Atenea virtual campus.