

## Course guide

### 270004 - IC - Introduction to Computers

Last modified: 30/01/2024

**Unit in charge:** Barcelona School of Informatics  
**Teaching unit:** 701 - DAC - Department of Computer Architecture.

**Degree:** BACHELOR'S DEGREE IN INFORMATICS ENGINEERING (Syllabus 2010). (Compulsory subject).

**Academic year:** 2023    **ECTS Credits:** 7.5    **Languages:** Catalan

#### LECTURER

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**Coordinating lecturer:** JOSEP-LLORENÇ CRUZ DIAZ - ENRIQUE MORANCHO LLENA

**Others:**

Primer quadrimestre:

OCTAVIO CASTILLO REYES - 31, 32, 41, 42, 43  
ANTONIO CORTÉS ROSSELLÓ - 21, 22, 23, 33, 71, 72, 73  
JOSEP-LLORENÇ CRUZ DIAZ - 11, 12, 13, 61, 62, 63  
MARC GONZÀLEZ TALLADA - 12, 42, 51, 52, 53, 63, 71, 72, 73  
JOSEP LARRIBA PEY - 21, 22, 23, 51, 52, 53  
EDUARDO TOMMY LOPEZ PASTOR - 11, 13, 31, 32, 33, 41, 43

Segon quadrimestre:

ANTONIO CORTÉS ROSSELLÓ - 11, 12  
JOSEP-LLORENÇ CRUZ DIAZ - 21  
MARC GONZÀLEZ TALLADA - 12  
JOSEP LARRIBA PEY - 11  
ENRIQUE MORANCHO LLENA - 21

#### PRIOR SKILLS

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Students should have acquired the skills expected of a student starting a bachelor's degree in Informatics.

#### DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

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**Specific:**

CT1.1B. To demonstrate knowledge and comprehension about the fundamentals of computer usage and programming. Knowledge about the structure, operation and interconnection of computer systems, and about the fundamentals of its programming.

CT6.2. To demonstrate knowledge, comprehension and capacity to evaluate the structure and architecture of computers, and the basic components that compound them.

**Generical:**

G6. SOLVENT USE OF THE INFORMATION RESOURCES: To manage the acquisition, structuring, analysis and visualization of data and information of the field of the informatics engineering, and value in a critical way the results of this management.

## TEACHING METHODOLOGY

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The teaching method for the subject is the Pygmalion method described by the Institute of Education Sciences of the UPC, summarised as 10 points (see Atenea for detailed information, as the course guide is merely a summary):

1. An ambitious final goal. Students will progress from knowing nothing of digital circuits or how they are built to designing a computer with all its details and 3,000 logic gates. This is an important motivational element.
2. A list of 100 specific learning objectives, describing what students should be able to do by the end of the course. These learning objectives are subject to assessment (students will know if they have achieved them or not) and there is an undertaking not to assess any learning objective not included in this list.
3. A detailed programme of activities for students to do in and (especially important) out of class. After each 2-hour theory/problem-solving class, students will spend a further 1.5 hours completing exercises (Moodle questionnaires for electronic delivery and other more complex exercises for hard-copy delivery) to be submitted at the beginning of the next class.
4. A step-by-step programme of activities. These will progressively cover the 100 specific learning objectives for the subject (the ambitious final goal is intended to be motivational and the step-by-step approach makes progress feasible).
5. Outcomes for each programmed activity embodied in the delivery of an assignment that shows whether the student has done the work. Students will be issued with the solutions to exercises and problems and with the quality criteria necessary to evaluate these assignments.
6. Timely feedback mechanisms based on assignment deliveries. Students and the lecturer can monitor progress as follows: 1) Students immediately know if a Moodle exercise solution is wrong and can resubmit as often as necessary until they get the right answer. 2) As feedback at the beginning of each class, doubts regarding the Moodle exercises and the written assignments done at home will be cleared up. 3) Students will complete exercises individually or in groups in class that will keep them informed on their progress. 4) Throughout the course, four theory/problem-solving and six laboratory exams/tests will be issued, for which timely feedback will be given.
7. Special activities for students with difficulties (and also for more advanced students): individual consultations, problem-solving workshops, etc.
8. Cooperative learning techniques to motivate students for the activities. Active learning techniques will be used in the theory classes to keep lecturer presentations short and ensure that students participate actively.
9. The grading method. This represents a further incentive to complete activities on time, learn and successfully complete the course.
10. Systematic data collection over the entire course. These data will be used to drive the continuous improvement process.

## LEARNING OBJECTIVES OF THE SUBJECT

- 1.Explain the operation of a von Neumann computer using their own words, including the internal structure in terms of processor subsystems, bus, storage, input/output and execution of a program in machine language, as well as the most important differences between the machine language of RISC and CISC computers.
- 2.Define the conventional numbering system in base  $b$  for representing natural numbers, particularly the binary case ( $b=2$ ), and also the system for representing integers in two's complement ( $Ca2$ ).
- 3.Explain natural number representation in base 2, 10 or 16 converted to another of these bases.
- 4.Explain a combinational logic circuit and specify the truth table for the basic logic gates (NOT, AND, OR and XOR) and the multiplexer and decoder blocks.
- 5.Analyse small combinational circuits (obtain truth tables and propagation time and create operational time schedules).
- 6.Synthesise small combinational circuits (obtain logic diagrams with one of the following sets of devices: NOT, AND and OR gates as a sum of minterms or minimum products), a decoder and OR gates, and a ROM and multiplexers.
- 7.Apply arithmetic algorithms to basic operations (addition, subtraction, comparison, multiplication and division by powers of two) with vectors of bits representing natural numbers in binary and integers in two's complement.
- 8.Draw the internal logic diagram for combinational blocks (combinational circuits that manipulate  $n$ -bit words) that perform basic arithmetic operations on natural numbers represented in binary and on integers represented in two's complement, as well as the internal logic block diagram that performs basic bitwise operations (NOT, AND, OR and XOR).
- 9.Explain sequential logic circuits (general Mealy and particular Moore cases) and specify the operation of an edge-triggered D-type flip-flop and depict its internal logic diagram using two multiplexers.
- 10.Analyse small Moore sequential circuits (obtain state graphs and minimum cycle time and draw simplified operational time schedules).
- 11.Synthesise small Moore sequential circuits (using the minimum number of edge-triggered D-type flip-flops and any of the combinational circuit synthesis techniques studied).
- 12.Design specific-purpose processors that manipulate  $n$ -bit words generated by a processing unit (designed ad hoc with combinational and sequential blocks) and a control unit (specified by a Moore state graph).
- 13.Explain the asynchronous four-phase handshaking communication protocol and apply it to data input/output in specific-purpose processors.
- 14.Draw the interconnection diagram for the general processing unit (GPU) at the block level and the internal logic diagram for each block (register bank and arithmetic logic unit).
- 15.Draw the Moore state graph for a specific-purpose control unit so that it implements specific functions along with the general processing unit (GPU).
- 16.Explain the steps necessary to transform a specific-purpose control unit (implementation of a state graph) into a general-purpose control unit which, together with the general processing unit (GPU), will form a simple RISC processor, and explain implicit sequencing and instruction coding.
- 17.Justify the need for a large data memory and explain the operation of a block of RAM by means of a schedule of its input and output signals (simplified model).
- 18.Depend the internal logic diagram for a simple input/output subsystem with keyboard and printer.
- 19.Depend an interconnection diagram for the storage and input/output subsystems with the processor (GCU+GPU) so as to configure a simple RISC computer.
- 20.Define, for each instruction to a simple RISC processor (some 20 instructions), format in machine language, syntax in assembly language and semantics (how the computer status is modified).
- 21.Indicate how computer status is modified (register content, data storage and I/O ports) after running small programs (maximum 10 instructions) written in simple RISC computer assembly language.
- 22.Writ

## STUDY LOAD

Type	Hours	Percentage
Hours large group	30,0	16.00
Hours small group	15,0	8.00
Self study	105,0	56.00
Hours medium group	30,0	16.00
Guided activities	7,5	4.00

**Total learning time:** 187.5 h

## CONTENTS

### Introduction

**Description:**

A brief introduction to digital information, digital information representation and digital circuits, special purpose processors, the Von Neumann machine, machine and assembly languages and their relationship to high-level languages (compilation/translation).

### Representing natural numbers

**Description:**

Representation of natural numbers in decimal and binary and generalisation to the conventional system in base  $b$ . Hexadecimal. Representation range. Range extension algorithm. Change of basis between conventional systems.

### Combinational logic circuits

**Description:**

Definition of a combinational logic circuit. Time schedules. Variables and logic functions. Truth tables. NOT, AND and OR logic gates. Logic circuit diagram. Interconnection rules for constructing valid combinational logic circuits. Logical analysis (from the diagram to the truth table). Synthesis (from the functional description to the truth table and from the truth table to the logic circuit): in sum of minterms with a decoder and OR gates, with a ROM and minimal sum of products using Karnaugh maps. Temporal analysis (time schedules and input-output propagation times).

### Natural numbers: combinational arithmetic blocks

**Description:**

Arithmetic algorithms for addition, subtraction, multiplication and division by powers of two natural numbers represented in binary. Full adder, half adder and full subtractor. Combinational blocks that implement the above arithmetic algorithms with detection results that cannot be represented in  $n$  bits. Comparators for equal, less and less or equal. Non-arithmetic combinational blocks (bitwise logical operators and tree multiplexer design). New arithmetic block design.

### Integers: representation and combinational arithmetic blocks

**Description:**

Representing integers. Two's complement. Range and range extension algorithm. Changing integer representation between sign and magnitude in the decimal system and two's complement. Arithmetic algorithms and implementing combinational blocks (with detection of results that cannot be represented in  $n$  bits): addition, sign change, subtraction, multiplication and division by powers of two and the less and less or equal comparators. Adder/subtractor with results detection that cannot be represented by natural numbers or integers.

### Sequential logical circuits

**Description:**

Memory needs and synchronisation. The clock signal. Definition of synchronous sequential circuit. Edge-triggered D-type flip-flops: definition and implementation with two multiplexers, time propagation and time schedules. Interconnection rules for constructing valid sequential circuits. Sequential circuit structures (Mealy and Moore models). Transition tables and output tables. State graphs for the Moore model. Simplified time schedules. Logic analysis: from the circuit to the state graph. Synthesis: from the functional specification to the state graph and from the state graph to the logic circuit diagram with a minimum number of flip-flops. Temporal analysis: critical paths and minimum cycle times.

### Special purpose processors

#### Description:

Introduction. Special-purpose processor design, with a processing unit (for n-bit words) and a control unit (generating the control word for each cycle). The processing unit is designed ad hoc using combinational and sequential blocks of n bits and the control unit is specified by a Moore state graph. Examples with synchronous data input/output: add four numbers, calculate the GCD of two numbers with the Euclidean algorithm, etc. Asynchronous communication protocol for data input/output: four-phase handshaking. Examples with asynchronous data input/output.

### General processing unit

#### Description:

Introduction: from special purpose to general purpose processors. Register bank with one write and two read buses. Arithmetic logic unit with bitwise functionality for logic operations, arithmetic operations (addition, subtraction, multiplication and division by powers of two for natural numbers and integers), comparators (equal, less and less or equal for natural numbers and integers) and movement. General processing unit (GPU) structure. Connections between the GPU and the control unit: control word and zero bit condition. Actions to implement in such problems using the GPU. Mnemonics of actions (AND, OR, XOR, NOT, ADD, SUB, SHA, SHL, CMPLT, CMPL, CMPEQ, CMPLTU, CMPL, MOV, IN, OUT and NOP) and associated control word bits. Actions with immediate values and actions that do not alter records. Special purpose processor design using the GPU (specifying the control unit via a state graph and the control word via mnemonics). Input/output address spaces and IN and OUT actions. Asynchronous data input/output via the four-phase handshaking protocol. Model designs based on high-level language code that specifies processor functionality (four-bit adder, GCD calculation for the Euclidean algorithm, etc.).

### General control unit

#### Description:

Initial implementation of the control unit (just like any other sequential circuit): with a state register, a ROM (where each word is stored in the next two possible states, depending on the Z-bit condition and the control word governing the GPU during a cycle) and a bus multiplexer to select the next state depending on Z. Von Neumann and Harvard computer models. ROM instruction storage. From the state graph to the program in machine/assembly language. Definitive control unit structure with implicit sequencing, 16-bit instructions and an instruction decoder to obtain the 50-bit control word from 16 instruction bits. SISA instructions format (with one, two or three registers) and coding. Uses: arithmetic, logical and comparative, sequence breaking, input-output, movement (register loading with a constant) and addition of a small constant. Examples of passing from graphs (specifying a control unit with specific objectives which executes an algorithm with the GPU) to code snippets in SISA assembly language so as to perform the same function (although usually requiring more cycles).

### Storage and input/output

#### Description:

RAM, a simple operational model (read and write schedules, access times for reading and set-up and signal pulse width permission to write scripts). Memory address space. Processor and data memory connections. Read (load: LD) and write instructions (store: ST): semantics, machine language format and assembler syntax. Examples of state modifications for specific load and store computer instructions. Examples of small programs with memory access. Simple input/output subsystem consisting of a keyboard and printer with the side effect of the state register (port) for data reading (keyboard) and data writing (printer) set to zero. Input/output with synchronisation by polling. Examples of small programs with data input/output data.

### Machine and assembly languages

#### Description:

General review of SISA machine and assembly language (25 instructions) as per the previous two topics. Exercises on: a) SISA code assembly and disassembly; b) computer state modification after execution of an instruction or small program; and c) writing small programs in assembly language.

### Single-cycle processors

**Description:**

Complete single-cycle implementation details (SISC Harvard unicycle) for a processor running programs in SISA machine language (as developed in topics 8, 9 and 10): a) minor GPU ALU modification to execute immediate instructions to move the largest 8-bits in a register to MOVHI; b) single address bus for the input/output space; and c) instruction decoder design to obtain a 46-bit control word from a 16-bit instruction using a small ROM and a small number of multiplexers and gates. ROM content of the instruction decoder. Temporary restrictions on write permission signals for storage and data input/output. Examples of changes to SISC Harvard unicycle design so that it executes a new instruction as well as the more than 25 original instructions. Calculating the critical path and minimum cycle time for a single-cycle computer. Small program run times.

### Multicycle processors

**Description:**

Introduction: justification for multicycle implementation (SISC Harvard multicycle) rather than single-cycle implementation (SISC Harvard unicycle). Changes to the processor control unit. Sequential control unit design: state graphs and their implementation. Temporary restrictions on write permission signals for storage and data input/output. Examples of changes to SISC Harvard multicycle design so that it executes a new instruction as well as the more than 25 original instructions. Calculating the critical path and minimum cycle time for a multicycle computer. Small program run times.

## ACTIVITIES

### Topics 1 and 2 theory/problem-solving classes

**Description:**

Participate actively in a two-hour explanatory-participatory theory/problem-solving class (2 hours). Home study of the assigned topic (1.5 hours). Complete the topic exercises for electronic delivery (Atenea questionnaires) and hard-copy delivery (at the beginning of each theory/problem-solving class) (1.5 hours).

**Specific objectives:**

1, 2, 3

**Full-or-part-time:** 5h

Theory classes: 1h

Practical classes: 1h

Self study: 3h

### Practical 0

**Description:**

Prepare the practical beforehand and complete a report for delivery at the start of the laboratory session (1.5 hours). Participate actively in laboratory sessions. Complete the pre-set test and the practical and complete and submit a final report (1 hour).

**Specific objectives:**

26

**Full-or-part-time:** 3h

Laboratory classes: 2h

Self study: 1h



### Practical 1

**Description:**

Prepare the practical beforehand and complete a report for delivery at the start of the laboratory session (3 hours). Participate actively in laboratory sessions. Complete the pre-set test and the practical and complete and submit a final report (2 hours).

**Specific objectives:**

26

**Full-or-part-time:** 5h

Laboratory classes: 2h

Self study: 3h

### L1

**Description:**

In laboratory session 1, practical 1 will be assessed on the basis of the previous session's report, the individual pre-set test (completed at the beginning of the session) and the final report. Learning objective 26 for the first part of topic 3 will be assessed. This will be done shortly after the four 2-hour theory/problem-solving classes, so that students have acquired the knowledge necessary to perform the practical.

**Specific objectives:**

26

### Topic 3 theory/problem-solving classes

**Description:**

Participate actively in three 2-hour explanatory-participatory theory/problem-solving classes (6 hours). Home study of the assigned topic (4.5 hours). Complete the topic exercises for electronic delivery (Atenea questionnaires) and hard-copy delivery (at the beginning of each theory/problem-solving class) (4.5 hours).

**Specific objectives:**

4, 5, 6

**Full-or-part-time:** 13h 30m

Theory classes: 3h

Practical classes: 3h

Self study: 7h 30m

### Topic 4 theory/problem-solving classes

**Description:**

Participate actively in two 2-hour explanatory-participatory theory/problem-solving sessions (4 hours). Home study of the assigned topic (3 hours). Complete the topic exercises for electronic delivery (Atenea questionnaires) and hard-copy delivery (at the beginning of each theory/problem-solving class) (3 hours).

**Specific objectives:**

7, 8

**Full-or-part-time:** 10h

Theory classes: 2h

Practical classes: 2h

Self study: 6h

### Topic 5 theory/problem-solving classes

**Description:**

Participate actively in a two-hour explanatory-participatory theory/problem-solving class (2 hours). Home study of the assigned topic (1.5 hours). Complete the topic exercises for electronic delivery (Atenea questionnaires) and hard-copy delivery (at the beginning of each theory/problem-solving class) (1.5 hours).

**Specific objectives:**

7, 8

**Full-or-part-time:** 5h

Theory classes: 1h

Practical classes: 1h

Self study: 3h

### Topic 6 theory/problem-solving classes

**Description:**

Participate actively in three 2-hour explanatory-participatory theory/problem-solving classes (6 hours). Home study of the assigned topic (4.5 hours). Complete the topic exercises for electronic delivery (Atenea questionnaires) and hard-copy delivery (at the beginning of each theory/problem-solving class) (4.5 hours).

**Specific objectives:**

9, 10, 11

**Full-or-part-time:** 15h

Theory classes: 3h

Practical classes: 3h

Self study: 9h

### Practical 2

**Description:**

Prepare the practical beforehand and complete a report for delivery at the start of the laboratory session (3 hours). Participate actively in laboratory sessions. Complete the pre-set test and the practical and complete and submit a final report (2 hours).

**Specific objectives:**

26

**Full-or-part-time:** 5h

Laboratory classes: 2h

Self study: 3h

### L2

**Description:**

In the laboratory session 2, practical 2 of the subject will be assessed on the basis of the previous session's report, the individual pre-set test (completed at the beginning of the session) and a final report. Learning objective 26 for topics 3, 4 and 6 will be assessed. This will be done shortly after the nine 2-hour theory/problem-solving classes, so that students have acquired the knowledge necessary to perform the practical.

**Specific objectives:**

26



### Topic 7 theory/problem-solving classes

**Description:**

Participate actively in two 2-hour explanatory-participatory theory/problem-solving sessions (4 hours). Home study of the assigned topic (3 hours). Complete the topic exercises for electronic delivery (Atenea questionnaires) and hard-copy delivery (at the beginning of each theory/problem-solving class) (3 hours).

**Specific objectives:**

12, 13

**Full-or-part-time:** 10h

Theory classes: 2h

Practical classes: 2h

Self study: 6h

### Practical 3

**Description:**

Prepare the practical beforehand and complete a report for delivery at the start of the laboratory session (3 hours). Participate actively in laboratory sessions. Complete the pre-set test and the practical and complete and submit a final report (2 hours).

**Specific objectives:**

26

**Full-or-part-time:** 5h

Laboratory classes: 2h

Self study: 3h

### L3

**Description:**

In laboratory session 3, practical 3 of the subject will be assessed on the basis of the previous session's report, the individual pre-set test (completed at the beginning of the session) and a final report. Learning objective 26 for the first part of topic 7 will be assessed. This will be done shortly after the twelve 2-hour theory/problem-solving classes, so that students have acquired the knowledge necessary to perform the practical.

**Specific objectives:**

26

### Recuperation of theory (if necessary) and completion of problems from topics 4, 5, 6 and 7

**Description:**

Participate actively in a two-hour problem-solving class (or theory recuperation if necessary) (2 hours).

**Specific objectives:**

7, 8, 9, 10, 11, 12, 13

**Full-or-part-time:** 3h

Practical classes: 1h

Self study: 2h

#### EP1

**Description:**

Theory/problem-solving exam 1 for continuous assessment, assessing all the learning objectives for topics 2 to 7.

**Specific objectives:**

1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13

**Full-or-part-time:** 2h

Guided activities: 2h

#### Resolution and group discussion of the evaluation act EP1.

**Description:**

The teacher will invite interested students to a presentation and discussion of the exam solutions, possible alternatives and typical mistakes made.

**Specific objectives:**

12, 14, 15

**Full-or-part-time:** 2h

Guided activities: 2h

#### Practical 4

**Description:**

Prepare the practical beforehand and complete a report for delivery at the start of the laboratory session (3 hours). Participate actively in laboratory sessions. Complete the pre-set test and the practical and complete and submit a final report (2 hours).

**Specific objectives:**

26

**Full-or-part-time:** 5h

Laboratory classes: 2h

Self study: 3h

#### L4

**Description:**

In laboratory session 4, practical 4 of the subject will be assessed on the basis of the previous session's report, the individual pre-set test (completed at the beginning of the session) and a final report. Learning objective 26 for the second part of topic 7 will be assessed (handshaking). This will be done shortly after the thirteen 2-hour theory/problem-solving classes, so that students have acquired the knowledge necessary to perform the practical.

**Specific objectives:**

26

### Topic 8 theory/problem-solving classes

**Description:**

Participate actively in three 2-hour explanatory-participatory theory/problem-solving classes (6 hours). Home study of the assigned topic (4.5 hours). Complete the topic exercises for electronic delivery (Atenea questionnaires) and hard-copy delivery (at the beginning of each theory/problem-solving class) (4.5 hours).

**Specific objectives:**

14, 15

**Full-or-part-time:** 15h

Theory classes: 3h

Practical classes: 3h

Self study: 9h

### Practice 5

**Description:**

Prepare the practical beforehand and complete a report for delivery at the start of the laboratory session (3 hours). Participate actively in laboratory sessions. Complete the pre-set test and the practical and complete and submit a final report (2 hours). Actively participate in the lab session. Make previous examination, perform practice and complete and submit the final report (2 hours).

**Specific objectives:**

26

**Full-or-part-time:** 5h

Laboratory classes: 2h

Self study: 3h

### L5

**Description:**

In laboratory session 5, practical 5 of the subject will be assessed on the basis of the previous session's report, the individual pre-set test (completed at the beginning of the session) and a final report. Learning objective 26 will be assessed for topics 3, 4 and 6. This will be done shortly after the fifteen 2-hour theory/problem-solving classes, so that students have acquired the knowledge necessary to perform the practical.

**Specific objectives:**

26

### Topic 9 theory/problem-solving classes

**Description:**

Participate actively in two 2-hour explanatory-participatory theory/problem-solving sessions (4 hours). Home study of the assigned topic (3 hours). Complete the topic exercises for electronic delivery (Atenea questionnaires) and hard-copy delivery (at the beginning of each theory/problem-solving class) (3 hours).

**Specific objectives:**

16, 20, 21

**Full-or-part-time:** 10h

Theory classes: 2h

Practical classes: 2h

Self study: 6h

### Topic 10 theory/problem-solving classes

**Description:**

Participate actively in two 2-hour explanatory-participatory theory/problem-solving sessions (4 hours). Home study of the assigned topic (3 hours). Complete the topic exercises for electronic delivery (Atenea questionnaires) and hard-copy delivery (at the beginning of each theory/problem-solving class) (3 hours).

**Specific objectives:**

17, 18, 19, 20, 21

**Full-or-part-time:** 10h

Theory classes: 2h

Practical classes: 2h

Self study: 6h

### Recuperation of theory (if necessary) and completion of problems for topics 8, 9 and 10

**Description:**

Participate actively in a 2-hour problem-solving class (or theory recuperation if necessary (4 hours).

**Specific objectives:**

14, 15, 16, 17, 18, 19, 20, 21, 22

**Full-or-part-time:** 4h

Theory classes: 1h

Practical classes: 1h

Self study: 2h

### Topic 11 theory/problem-solving classes

**Description:**

Participate actively in a 2-hour explanatory-participatory theory/problem-solving class (2 hours). Home study of the assigned topic (1.5 hours). Complete the topic exercises for electronic delivery (Atenea questionnaires) and hard-copy delivery (at the beginning of each theory/problem-solving class) (1.5 hours).

**Specific objectives:**

20, 21, 22

**Full-or-part-time:** 5h

Theory classes: 1h

Practical classes: 1h

Self study: 3h

### Topic 12 theory/problem-solving classes

**Description:**

Participate actively in two 2-hour explanatory-participatory theory/problem-solving sessions (4 hours). Home study of the assigned topic (3 hours). Complete the topic exercises for electronic delivery (Atenea questionnaires) and hard-copy delivery (at the beginning of each theory/problem-solving class) (3 hours).

**Specific objectives:**

23, 24, 25

**Full-or-part-time:** 11h

Theory classes: 2h

Practical classes: 2h

Self study: 7h

### Practical 6

**Description:**

Prepare the practical beforehand and complete a report for delivery at the start of the laboratory session (3 hours). Participate actively in laboratory sessions. Complete the pre-set test and the practical and complete and submit a final report (3 hours).

**Specific objectives:**

26

**Full-or-part-time:** 6h

Laboratory classes: 3h

Self study: 3h

### L6

**Description:**

In laboratory session 6, practical 6 of the subject will be assessed on the basis of the previous session's report, the individual pre-set test (completed at the beginning of the session) and a final report. Learning objective 26 will be assessed for topics 11 and 12. This will be done shortly after the twenty 2-hour theory/problem-solving classes, so that students have acquired the knowledge necessary to perform the practical.

**Specific objectives:**

26

### Topic 13 theory/problem-solving classes

**Description:**

Participate actively in two 2-hour explanatory-participatory theory/problem-solving sessions (4 hours). Home study of the assigned topic (3 hours). Complete the topic exercises for electronic delivery (Atenea questionnaires) and hard-copy delivery (at the beginning of each theory/problem-solving class) (3 hours).

**Specific objectives:**

23, 24, 25

**Full-or-part-time:** 11h 30m

Theory classes: 2h

Practical classes: 2h

Self study: 7h 30m

### Recuperation of theory (if necessary) and completion of problems from topics 11, 12 and 13

**Description:**

Participate actively in three 2-hour participatory problem-solving classes (or theory recuperation if necessary).

**Specific objectives:**

20, 21, 22, 23, 24, 25

**Full-or-part-time:** 8h

Practical classes: 4h

Self study: 4h

### EP2

**Description:**

Theory/problem-solving exam 2 for continuous assessment, assessing all the learning objectives for topics 8 to 14.

**Specific objectives:**

14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25

**Full-or-part-time:** 3h

Guided activities: 3h

### Resolution and group discussion of the evaluation act EP2.

**Description:**

The teacher will invite interested students to a presentation and discussion of the exam solutions, possible alternatives and typical mistakes made.

**Specific objectives:**

21, 22, 23, 24, 25

**Full-or-part-time:** 2h 30m

Guided activities: 2h 30m

### Task to evaluate the transferable competency referring to sound use of information resources

**Description:**

Task completion (8 hours).

**Specific objectives:**

28

**Related competencies :**

G6. SOLVENT USE OF THE INFORMATION RESOURCES: To manage the acquisition, structuring, analysis and visualization of data and information of the field of the informatics engineering, and value in a critical way the results of this management.

**Full-or-part-time:** 8h

Self study: 8h

### Final Exam

**Description:**

Final exam in which all learning objectives for all the topics will be assessed. It is not necessary for students to sit this exam as they can obtain the maximum final mark via continuous assessment of the theory/problem-solving sessions (80% of NTP) and laboratory sessions (20% of NL). For students who have not passed via continuous assessment, the final exam mark may be replaced by the theory/problem-solving mark obtained via continuous assessment. Students who have passed but who want to improve their mark may request to do the exam by informing the course coordinator at least a week in advance.

**Specific objectives:**

1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25

## GRADING SYSTEM

The final mark (NF) is computed from the theory/problem-solving mark (NTP) and the laboratory mark (NL) following this formula:

$$NF = 0.8 \text{ NTP} + 0.2 \text{ NL}$$

Theory/problem-solving mark (NTP) for continuous assessment:

The NTP can be obtained through continuous assessment or through the Final Exam. The course is planned in such a way that it can be passed by continuous assessment. However, if a student cannot participate in the activities required by the continuous assessment (or if the student fails to pass the continuous assessment), he/she can obtain the NTP grade directly from the Final Exam (EF). The Theory and Problems Mark (NTP) for continuous assessment is computed with the marks of the 2 partial exams (NP1 and NP2) together with the deliverables and assignments indicated by the professor. The NTP grade is computed as follows:

$$NTP = \text{maximum}(0.4 \cdot NP1 + 0.6 \cdot NP2, EF).$$

Laboratory mark (NL):

The NL mark is based on the average of the six laboratory sessions (practical 0 is not considered). The mark for each laboratory NLi (NLi for i = 1 ... 6) is calculated using the following formula:

If a complete initial report is delivered at the beginning of the session,  $NLi = 0.65 \times PPI + 0.35 \times IFi$  (otherwise  $NLi = 0$ ).

Where:

PPI is the mark for the individual pre-test (about 15 minutes long) performed at the beginning of the session. The pre-test consists of questions similar to those in the initial report.

IFi is the mark for the final report completed during the laboratory session.

REEVALUATION.

This course has reevaluation. You may check the school's information on reevaluation at <https://www.fib.upc.edu/en/reavaluacions-gei>. Students signing in for reevaluation have to fulfill the general requirements plus (1) a final score of 2.5 or higher in both the continuous evaluation and in the final exam; and (2) not participating or not having the minimum score will result in the inadmissibility to the reevaluation.

## BIBLIOGRAPHY

**Basic:**

- Navarro, J.J.; Juan, T. Introducción a los computadores.
- Navarro, J.J. Introducción a los computadores: prácticas. CPET,
- Navarro, J.J.; Muntés Mulero, V.; Llorenç Cruz, J.; Palomar, Ó.; Sánchez Castaño, F.; Solé, M. Introducció als computadores: col·lecció de problemes. CPET,

**Complementary:**

- Gajski, D.D. Principios de diseño digital. Prentice Hall, 1997. ISBN 8483220040.



## RESOURCES

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**Hyperlink:**

- <http://atenea.upc.edu>