Course guide
270062 - MP - Multiprocessors

Last modified: 30/01/2024

Unit in charge: Barcelona School of Informatics
Teaching unit: 701 - DAC - Department of Computer Architecture.

Degree: BACHELOR'S DEGREE IN INFORMATICS ENGINEERING (Syllabus 2010). (Optional subject).

Academic year: 2023 **ECTS Credits:** 6.0 **Languages:** Spanish

LECTURER

Coordinating lecturer: JOSE M. LLABERIA GRIÑÓ

Others: Primer quadrimestre:
JOSE M. LLABERIA GRIÑÓ - 10

Segon quadrimestre:
JOSE M. LLABERIA GRIÑÓ - 10

PRIOR SKILLS

The subjects listed in IC, EC, EP, AC, PAR, AC2

REQUIREMENTS

- Prerequisite AC2
- Prerequisite PAR

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
CEC2.1. To analyse, evaluate, select and configure hardware platforms for the development and execution of computer applications and services.
CEC3.2. To develop specific processors and embedded systems; to develop and optimize the software of these systems.
CT6.2. To demonstrate knowledge, comprehension and capacity to evaluate the structure and architecture of computers, and the basic components that compound them.
CT7.1. To demonstrate knowledge about metrics of quality and be able to use them.

Generical:
G7. AUTONOMOUS LEARNING: to detect deficiencies in the own knowledge and overcome them through critical reflection and choosing the best actuation to extend this knowledge. Capacity for learning new methods and technologies, and versatility to adapt oneself to new situations.

TEACHING METHODOLOGY

Classes theory in which concepts are developed and there is student participation.
Classes of problems which apply the concepts developed in the theory classes and is an active student.
Laboratory classes in which to apply the concepts developed in theory class a concrete example of multiprocessor. The active agent is pupils and collaboration between elements of the group is the means to increase and consolidate knowledge.
The course is developed constructively. In other words, is part of the concepts learned in previous courses in each subject and the subject of increased knowledge and ability to understand, analyze and reason about aspects of a multiprocessor. This training is more quantitative.

LEARNING OBJECTIVES OF THE SUBJECT

1.Training to understand the basic concepts in multiprocessors: terminology, organization, elements of a Multiprocessor, consistency and coherence in memory.
2.Training to understand the basic concepts of communication and synchronization in a multiprocessor.
3.Training to understand the constraints imposed by technology, through the operation of ideal solutions adopted and implemented a multiprocessor.
4.Capacity to analyze and critically evaluate a multiprocessor and its elements.
5.Training for the use of a hardware description language and its application in the specification of elements of a Multiprocessor

STUDY LOAD

Type	Hours	Percentage
Hours small group	15,0	10.00
Guided activities	6,0	4.00
Hours medium group	15,0	10.00
Hours large group	30,0	20.00
Self study	84,0	56.00

Total learning time: 150 h

CONTENTS

Motivation

Description:
Obstacles exist to exploit the parallelism at the level of instruction. Increased productivity of a multithreaded processor using the technique. Use the available number of transistors on a chip using the technique of replication of processors.

Consistency and coherence of memory

Description:
Concepts of memory consistency and cache coherency. Memory model specified in the machine language. Need to maintain consistency among copies of data.

Multiprocessor core

Description:
Elements of a multiprocessor system. Private Cache. Interconnection Network: Support for a model of consistency. Coherence cache.

Communication and synchronization

Description:
Support the machine language for communication and synchronization. Basic mechanisms of synchronization.

Small-scale multiprocessor

Description:
Increased performance. Reduction of bandwidth required. Cache.Multiprocesador coherence protocols on a chip.

Scalable multiprocessor

Description:
Implications of the number of processors in a multiprocessor architecture. Interconnection of several chip multiprocessor.

ACTIVITIES

Consolidation

Description:
Final exam. Evaluation of all the objectives of the course.

Specific objectives:
1, 2, 3, 4, 5

Related competencies :
G7. AUTONOMOUS LEARNING: to detect deficiencies in the own knowledge and overcome them through critical reflection and choosing the best actuation to extend this knowledge. Capacity for learning new methods and technologies, and versatility to adapt oneself to new situations.

Full-or-part-time: 11h
Guided activities: 3h
Self study: 8h

Test

Description:
Evaluation goal for the first three issues.

Specific objectives:
1, 4, 5

Related competencies :
G7. AUTONOMOUS LEARNING: to detect deficiencies in the own knowledge and overcome them through critical reflection and choosing the best actuation to extend this knowledge. Capacity for learning new methods and technologies, and versatility to adapt oneself to new situations.

Full-or-part-time: 12h
Guided activities: 2h
Self study: 10h

Motivation

Description:
To study the theoretical concepts of the subject and resolve financial problems and proposed.

Specific objectives:
1, 4, 5

Related competencies :
G7. AUTONOMOUS LEARNING: to detect deficiencies in the own knowledge and overcome them through critical reflection and choosing the best actuation to extend this knowledge. Capacity for learning new methods and technologies, and versatility to adapt oneself to new situations.

Full-or-part-time: 12h
Theory classes: 3h
Practical classes: 2h
Laboratory classes: 1h
Self study: 6h

Consistency and coherence of memory

Description:
To study the theoretical concepts of the subject and resolve financial problems and proposed.

Specific objectives:
1, 5

Related competencies :
G7. AUTONOMOUS LEARNING: to detect deficiencies in the own knowledge and overcome them through critical reflection and choosing the best actuation to extend this knowledge. Capacity for learning new methods and technologies, and versatility to adapt oneself to new situations.

Full-or-part-time: 21h
Theory classes: 4h
Practical classes: 2h
Laboratory classes: 3h
Self study: 12h

Multiprocessor core

Description:
To study the theoretical concepts of the subject and resolve financial problems and proposed.

Specific objectives:
1, 4, 5

Related competencies :
G7. AUTONOMOUS LEARNING: to detect deficiencies in the own knowledge and overcome them through critical reflection and choosing the best actuation to extend this knowledge. Capacity for learning new methods and technologies, and versatility to adapt oneself to new situations.

Full-or-part-time: 29h
Theory classes: 6h
Practical classes: 3h
Laboratory classes: 4h
Self study: 16h

Communication and synchronization

Description:
To study the theoretical concepts of the subject and resolve financial problems and proposed.

Specific objectives:
2, 5

Related competencies :
G7. AUTONOMOUS LEARNING: to detect deficiencies in the own knowledge and overcome them through critical reflection and choosing the best actuation to extend this knowledge. Capacity for learning new methods and technologies, and versatility to adapt oneself to new situations.

Full-or-part-time: 19h
Theory classes: 4h
Practical classes: 2h
Laboratory classes: 3h
Self study: 10h

Small-scale multiprocessor

Description:
To study the theoretical concepts of the subject and resolve financial problems and proposed.

Specific objectives:
3, 5

Full-or-part-time: 27h
Theory classes: 5h
Practical classes: 4h
Laboratory classes: 4h
Self study: 14h

Scalable multiprocessor

Description:
To study the theoretical concepts of the subject and resolve financial problems and proposed.

Specific objectives:
3, 4

Full-or-part-time: 19h
Theory classes: 3h
Practical classes: 2h
Self study: 14h

Consolidation

Description:
Consolidation of concepts developed during the course.

Specific objectives:
1, 2, 3, 4, 5

Related competencies :
G7. AUTONOMOUS LEARNING: to detect deficiencies in the own knowledge and overcome them through critical reflection and choosing the best actuation to extend this knowledge. Capacity for learning new methods and technologies, and versatility to adapt oneself to new situations.

GRADING SYSTEM

Proof (P): Written test which evaluated the goal for the first three issues.
Final exam (F): Written test which evaluated all the objectives of the course.
Laboratory (L) is evaluated based on reports submitted in each of the sessions and, if appropriate, a personal interview.

The final (NF) is calculated using the following expression:
NF = max (0.8 x F (0.65 x F + 0.15 P)) + 0.2 x L

The level of achievement of generic competition evaluated indirectly from the notes of evidence and the final exam.
The corresponding note is:
A if 8.5 =

BIBLIOGRAPHY

Basic:
- Culler, D.E.; Singh, J.P.; Gupta, A. Parallel computer architecture: a hardware/software approach. Morgan Kaufmann Publishers, 1999. ISBN 1-55860-343-3.
- Capilano Computing Systems. LogicWorks 5: interactive circuit design software. Prentice Hall, 2004. ISBN 9780131456587.