Course guide
330220 - SD - Digital Systems

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Unit in charge: Manresa School of Engineering
Teaching unit: 750 - EMIT - Department of Mining, Industrial and ICT Engineering.

Degree: BACHELOR'S DEGREE IN ICT SYSTEMS ENGINEERING (Syllabus 2010). (Compulsory subject).

Academic year: 2023 **ECTS Credits:** 6.0 **Languages:** Catalan

LECTURER

Coordinating lecturer: Bonet Dalmau, Jordi

Others: Arumi Casanovas, Arnau

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
1. (ENG) L'assignatura contribueix a desenvolupar:
- La capacitat d'especificar, analitzar, dissenyar, avaluar i documentar circuits digitals, tant seqüencials com combinacionals, així com les seves alternatives d'implementació, incloent dispositius CPLD i FPGA.
- La capacitat d'emprar les eines i els llenguatges d'especificació, síntesi i verificació de circuits digitals.
- El coneixement i la capacitat d'emprar les eines i la instrumentació existents per a l'anàlisi, el disseny, el desenvolupament i la verificació de sistemes electrònics, informàtics i de comunicacions.
2. The ability to use tools and languages specification, synthesis and verification of digital circuits.
3. Knowledge and ability to use existing tools and instrumentation for the analysis, design, development and verification of electronic, computer and communications systems.

Transversal:
4. THIRD LANGUAGE. Learning a third language, preferably English, to a degree of oral and written fluency that fits in with the future needs of the graduates of each course.
5. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 1. Planning oral communication, answering questions properly and writing straightforward texts that are spelt correctly and are grammatically coherent.

TEACHING METHODOLOGY

The subject consists of face-to-face activities consisting of 3 hours per week of class and 2 hours per fortnight of laboratory practices.
The student carries out learning through various mechanisms. In the lectures and participative classes the contents of the subject are presented and the interaction between students and teacher is facilitated. Individual / group personal work activities are also proposed to contribute to the understanding of the subject.
In laboratory classes, students carry out preliminary work that helps to put into context the work that is intended to be carried out in the laboratory. The laboratory activity itself is carried out in groups of two students and allows experimenting with certain aspects developed in the subject. The writing of the memory and the interaction with the teacher in the laboratory allows working on the oral and written communication skills.
Periodically, the teacher will give a class in English where a summary of the content previously introduced in the subject will be presented. In the event that the student has any doubts, the question will also have to be formulated in English.

LEARNING OBJECTIVES OF THE SUBJECT

Upon completion of the Digital Systems course, the student:

- Understand the foundations of programmable devices (CPLD, FPGA) and analyze, design, and implement general, moderately complex digital circuits.
- Write simple technical reports and present them orally.

STUDY LOAD

Type	Hours	Percentage
Self study	90,0	60.00
Hours large group	45,0	30.00
Hours small group	15,0	10.00

Total learning time: 150 h

CONTENTS

1. INTRODUCTION TO PROGRAMMABLE DEVICES

Description:
This topic presents digital design alternatives and when programmable devices (CPLD, FPGA) are the best design option. Different methods for describing digital hardware will be outlined as well. VHDL will be primarily used in the class.

Related activities:
All.

Full-or-part-time: 11h
Theory classes: 3h
Laboratory classes: 2h
Self study : 6h

2. HIGH DENSITY PROGRAMMABLE DEVICES

Description:
In this topic, the aim is for students to:
- Understand and remember the main programmable digital elements and identify the different architectures and features of a device by reading its datasheet.
- Search for the best design option (speed, consumption, etc.) among manufacturers and components.
- Understand the specifications of a real assembly based on a CPLD/FPGA and apply them.

Related activities:
All.

Full-or-part-time: 46h
Theory classes: 14h
Laboratory classes: 4h
Self study : 28h

3. DIGITAL DESIGN BASED ON PROGRAMMABLE DEVICES AND VHDL

Description:
In this topic, the aim is for students to:
- Understand and remember the main digital building blocks and their definition in VHDL.
- Design moderately complex digital systems and create the stimuli required to ensure they operate properly.
- Study simple protocols for commercial devices and implement the digital hardware needed to communicate with these devices.
- Understand the basic modules that make up a simple computer and how assembly instructions are executed.

Related activities:
All.

Full-or-part-time: 93h
Theory classes: 28h
Laboratory classes: 9h
Self study : 56h

ACTIVITIES

1. MASTER AND PARTICIPATORY CLASSES

Description:
Theoretical content will be presented during these sessions. Students will have the opportunity to participate and interact with the professor.

Specific objectives:
- Know how to design digital circuits described in VHDL and recognize the basic digital blocks associated with this VHDL description.
- Know how to design the stimuli that allow to verify a digital circuit.
- Understand the specification sheets of commercial programmable devices.
- Understand a simple real protocol and know how to implement it with digital machinery.
- Know and know what it takes to put a programmable device (CPLD, FPGA) into practice.

Material:
Published teaching material.
Recommended bibliography.

Delivery:
Occasionally some evaluable activity is performed, contributing a proportional part to an EXE variable.

Full-or-part-time: 40h
Theory classes: 40h

2. LABORATORY CLASSES

Description:
Practicals lasting two hours will be held at the laboratory every two weeks and will be completed in pairs. The practical worksheet will be available on Atenea before the session. A computer with the software needed to simulate digital components will be available at the lab. The equipment required to experiment with commercial digital devices will also be available. The professor will give students individual feedback on their progress. At the end of each practical, the groups will email the practical professor a file in which they comment on the work they have completed and knowledge they have gained.

Specific objectives:
- Implement digital circuits based on FPGA and VHDL in the laboratory.
- Validate the operation of both simulated and physical digital circuits.
- Write and present documents reflecting the design and validation process of digital circuits.

Material:
Electronic equipment, breadboard, digital devices, computer with adequate software. Development board based on FPGA.
Statement of the practice and support information to carry out the work.

Delivery:
Before carrying out the practice, the students will deliver the previous individual study corresponding to the practice to be carried out.
During the session, the achievement of the objectives of each laboratory session will be assessed, taking into account the degree of understanding of the work demonstrated for each student.
At the end of the session, each working group will prepare a final report that reflects the main aspects of the work carried out.
The grade obtained in these activities configures the LAB variable.

Full-or-part-time: 25h
Laboratory classes: 15h
Self study: 10h

3. INDIVIDUAL / GROUP PERSONAL WORK

Description:
Students must complete certain activities on their own time in order to achieve the objectives of the subject.

Specific objectives:
All of the subject.

Material:
Published teaching material.
Recommended bibliography.

Delivery:
The individual / group personal work will be translated, in part, to the completion of exercises during the course. The grading of these exercises will contribute to the EXE variable.

Full-or-part-time: 50h
Self study: 50h

4. EXAMS

Description:
Students must complete certain activities on their own time in order to achieve the objectives of the subject. There will be a midterm that students must take individually. At the end of the class, there will be a final exam on the overall knowledge acquired.

Material:
Test statements.

Delivery:
The control test score sets the variable CON.
The final test grade sets the FIN variable.

Full-or-part-time: 35h
Theory classes: 5h
Self study: 30h

GRADING SYSTEM

The final mark for the class will be calculated using the following equation:
Final mark = 0.15 * EXE + 0.20 * CON + 0.25 * LAB + 0.40 * FIN

Note 1. If the final exam mark is greater (in part or in total) than other aspects assessed, it will substitute the results obtained on other activities during the class.
Note 2. If the marks obtained on individual activities are substantially lower than those obtained on group activities, students may be requested to complete individual activities similar to those completed in group. The marks on these individual activities will replace the group ones.

EXAMINATION RULES.

In the case of laboratory activities for which a previous study has been established, it will be mandatory to submit it before accessing the laboratory.
Those activities that are explicitly declared as individual, whether in person or not, will be carried out without any collaboration from other people.
The dates, formats and other delivery conditions established will be mandatory.

BIBLIOGRAPHY

Basic:
- Ashenden, Peter J. Digital design: an embedded systems approach using VHDL [on line]. Burlington, MA: Morgan Kaufmann Publishers, 2007 [Consultation: 31/05/2022]. Available on: https://ebookcentral-proquest-com.recursos.biblioteca.upc.edu/lib/upcatalunya-ebooks/detail.action?docID=858615. ISBN 9780123695284.
- Katz, Randy H.; Boriello, Gaetano. Contemporary logic design. 2nd ed. Upper Saddle River: Pearson Educational International, 2005. ISBN 0131278304.