Course guide
330229 - ACO - Computer Architecture

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Unit in charge: Manresa School of Engineering
Teaching unit: 750 - EMIT - Department of Mining, Industrial and ICT Engineering.

Degree: BACHELOR'S DEGREE IN ICT SYSTEMS ENGINEERING (Syllabus 2010). (Compulsory subject).

Academic year: 2023 **ECTS Credits:** 6.0 **Languages:** Catalan

LECTURER

Coordinating lecturer: ANTONI ESCOBET CANAL

Others:

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
1. Basic knowledge of the use and programming of computers, operating systems, databases and computer programs with application in engineering.
2. Knowledge and understanding of the architecture of programmable devices, including the identification of the elements that make it up and their interaction, with emphasis on the most common architectures of embedded systems.
3. The knowledge and ability to use existing tools and instrumentation for the analysis, design, development and verification of electronic, computer and communications systems.
4. Develop their ability to solve real problems through the development of small and medium-sized programs at the industrial level.

Transversal:
5. THIRD LANGUAGE. Learning a third language, preferably English, to a degree of oral and written fluency that fits in with the future needs of the graduates of each course.
6. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 2. Using strategies for preparing and giving oral presentations. Writing texts and documents whose content is coherent, well structured and free of spelling and grammatical errors.

TEACHING METHODOLOGY

The course consists of face-to-face activities consisting of 2 hours per week of class and 2 hours of laboratory practices.
The student carries out learning through various mechanisms. In the lectures and participative classes the contents of the subject are presented and the interaction between students and teacher is facilitated. Individual / group personal work activities are also proposed that should contribute to the understanding of the subject.
In laboratory classes, students carry out preliminary work that helps to put into context the work that is intended to be carried out in the laboratory. The laboratory activity itself is developed in groups of two students and allows experimenting with certain aspects of the subject. The writing of the memory and the interaction with the teacher in the laboratory allows working on the oral and written communication skills.
Periodically, the teacher will give a class in English where a summary of the content previously introduced in the subject will be presented. In case the student has any doubts, the question must also be formulated in English.

LEARNING OBJECTIVES OF THE SUBJECT

At the end of the Computer Architecture course, the student:

- Design different memory structures and recognize the different types that exist.
- Understand the structure and architecture of a commercial microprocessor.
- Design systems based on a commercial microprocessor.
- Perform standard digital communication.
- Understand what advanced architectures are.
- Write simple technical reports and present them orally.

STUDY LOAD

Type	Hours	Percentage
Hours large group	45,0	30.00
Self study	90,0	60.00
Hours small group	15,0	10.00

Total learning time: 150 h

CONTENTS

1. INTRODUCTION

Description:
This topic presents different architectures and a brief description of their history.

Related activities:
All.

Full-or-part-time: 5h
Theory classes: 3h
Self study : 2h

2. STRUCTURE AND PROGRAMMING OF A MICROPROCESSOR

Description:
This topic presents the structure of a commercial microprocessor (registers, process units, control unit, buses, etc.), the assembly language with its instruction set architecture, and interruptions. Different addressing modes and data transfer techniques (by polling and by interruptions) are presented. Implementation of basic programming schemas: conditionals, iterations, and subroutines. Applications. Advanced architectures.

Related activities:
All.

Full-or-part-time: 74h
Theory classes: 20h
Laboratory classes: 8h
Self study : 46h

3. MEMORIES

Description:
This topic describes different types of memory and their hierarchy and control within a computer.

Related activities:
All.

Full-or-part-time: 31h
Theory classes: 10h
Laboratory classes: 3h
Self study : 18h

4. CONTROLLERS OF A COMPUTER

Description:
This topic touches on the different essential drivers in a computer. The bus arbiter, the data transfer driver via direct memory access, and the interrupt handler.

Related activities:
All.

Full-or-part-time: 20h
Theory classes: 6h
Laboratory classes: 2h
Self study : 12h

5. COMMUNICATIONS BUSES

Description:
This topic presents both internal and external communication buses. PCI buses and USBs are explained in detail.

Related activities:
All.

Full-or-part-time: 20h
Theory classes: 6h
Laboratory classes: 2h
Self study : 12h

ACTIVITIES

TITLE OF ACTIVITY 1: LECTURES WITH PARTICIPATION

Description:
Theoretical content will be presented during these sessions. Students will have the opportunity to participate and interact with the professor.

Specific objectives:
- Understand the operation of the microprocessor.
- Know how to choose the best device for each particular case.
- Know the programming tools.
- Know and know what it takes to put a programmable device into practice.

Material:
Published teaching material.
Recommended bibliography.

Delivery:
Occasionally some evaluable activity will be carried out, which will contribute in a proportional part to the EXE variable.

Full-or-part-time: 41h
Theory classes: 41h

TITLE OF ACTIVITY 2: LABORATORY SESSIONS

Description:
Practicals lasting two hours will be held at the laboratory every two weeks and will be completed in pairs. The practical worksheet will be available on Atenea before the session. A computer with the software needed to simulate the programmes developed will be available at the lab. The equipment required to experiment with commercial devices will also be available. The professor will give students individual feedback on their progress. At the end of each practical, the groups will upload a file to Atenea in which they comment on the work they have completed and knowledge they have gained.

Specific objectives:
- Experiment on computer architectures.
- Write and present documents reflecting the design and validation process of digital circuits.

Material:
Electronic equipment, breadboard. Statement of the practice and supporting information to carry out the work.

Delivery:
Before carrying out the practice, the students will deliver the previous individual study corresponding to the practice to be carried out.
During the session, the achievement of the objectives of each laboratory session will be assessed, taking into account the degree of understanding of the work demonstrated by each student.
At the end of the session, each working group will prepare a final report that reflects the main features of the actual work.
The grade obtained in these activities configures the LAB variable.

Full-or-part-time: 45h
Laboratory classes: 15h
Self study: 30h

TITLE OF ACTIVITY 3: INDIVIDUAL / GROUP WORK

Description:
Students must complete certain activities on their own time in order to achieve the objectives of the subject.

Specific objectives:
All of the subject.

Material:
Published teaching material.
Recommended bibliography.

Delivery:
Individual / group personal work will be translated, in part, into exercises during the course. The grading of these exercises will contribute to the EXE variable.

Full-or-part-time: 30h
Self study: 30h

TITLE OF ACTIVITY 4: EXAMS

Description:
There will be a midterm that students must take individually. At the end of the class, there will be a final exam on the overall knowledge acquired.

Material:
Test statements.

Delivery:
The control test score sets the variable CON.
The final test grade sets the FIN variable.

Full-or-part-time: 34h
Theory classes: 4h
Self study: 30h

GRADING SYSTEM

The qualification is made based on 3 elements:

1. Assessment of students' independent work (EX + CON). This includes progress made in both theoretical and practical aspects. It will be calculated based on the mandatory exercises delivered during the year and mid-term exams.
2. The evaluation of the practical work (P). It is carried out from the delivery of the practices that are carried out during the course.
3. The final evaluation (END). It is done through a final exam that is global in nature and integrates all the theoretical knowledge and skills acquired during the course.

From these elements the final grade is calculated with the following weightings: Final grade = 0.3 * (EXE + CON) + 0.3 * LAB + 0.4 * END

EXAMINATION RULES.

In the case of laboratory activities for which a previous study has been established, it will be mandatory to submit it before accessing the laboratory.
Those activities that are explicitly declared as individual, whether in person or not, will be carried out without any collaboration from other people.
The dates, formats and other delivery conditions that are established will be mandatory.

BIBLIOGRAPHY

Basic:
- García Carballeira, Félix; et al. Problemas resueltos de estructura de computadores. Madrid: Paraninfo, 2015. ISBN 9788428337014.
- Stallings, William. Organización y arquitectura de computadores [on line]. 7ª ed. Madrid: Prentice-Hall, 2006 [Consultation: 02/06/2022]. Available on: https://www-ingebook-com.recursos.biblioteca.upc.edu/ib/NPcd/IB_BooksVis?cod_primaria=1000187&codigo_libro=1266. ISBN 9788489660823.
- Patterson, David A.; Hennessy, John L. Estructura y diseño de computadores [on line]. 4ª ed. Barcelona: Reverté, 2011 [Consultation: 27/05/2022]. Available on: https://ebookcentral-proquest-com.recursos.biblioteca.upc.edu/lib/upcatalunya-ebooks/detail.action?docID=5635431. ISBN 9788429126204.
- Manual de referència i notes d'aplicació del fabricant.
- Patterson, David A.; Hennessy, John L. Computer organization and design: the hardware/software interface. 4th ed. Amsterdam: Elsevier Morgan Kaufmann, 2009. ISBN 9780123744937.
- Nisan, Noam; Schocken, Shimon. The elements of computing systems: building a modern computer from first principles. London: MIT Pres, 2005. ISBN 9780262640688.
- Furber, Stephen B. ARM system-on-chip architecture. 2nd ed. Harlow: Addison-Wesley, 2000. ISBN 9780201675191.