Course guide
340375 - ESC2-I3O01 - Computer Structure II

Last modified: 23/05/2025

Unit in charge: Vilanova i la Geltrú School of Engineering
Teaching unit: 701 - DAC - Department of Computer Architecture.

Degree: BACHELOR'S DEGREE IN INFORMATICS ENGINEERING (Syllabus 2018). (Compulsory subject).

Academic year: 2025 **ECTS Credits:** 6.0 **Languages:** Catalan, Spanish

LECTURER

Coordinating lecturer: Marin Tordera, Eva

Others: Heredero Lazaro, Ana M.
Marin Tordera, Eva

REQUIREMENTS

Introduction to Computers
Computer Structure I

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
1. CEFC1. Ability to design, develop, select and value applications and informatic systems affirming its reliability, security and quality corresponding to ethical principals and legislation and current rules.
2. CEFC13. Knowledge and application of necessary tools for storage, processing and access to informatic systems, including the ones based on webs.
3. CEFC4. Ability to work out technical conditions of an informatic installation observing standard and current rules.
4. CEFC7. Knowledge, design and efficient use of data types and structures the most appropriate to resolve problems.
5. CEFC9. Ability to know, understand and assess computer structure and architecture, as well as basic components forming them.

Transversal:
6. THIRD LANGUAGE. Learning a third language, preferably English, to a degree of oral and written fluency that fits in with the future needs of the graduates of each course.
7. SUSTAINABILITY AND SOCIAL COMMITMENT - Level 2. Applying sustainability criteria and professional codes of conduct in the design and assessment of technological solutions.

TEACHING METHODOLOGY

LEARNING OBJECTIVES OF THE SUBJECT

Deeper knowledge of the structure of computers, as well as in the design and implementation of small micro-computer based systems. Specifically, it aims to understand and delve into the internal structures and the memory hierarchy (disk, main memory, caches, mechanisms for error detection and correction) in the concepts of concurrency, input / output and buses (survey, interruptions, DMA, types of I / S), and its integration as part of an operating system

STUDY LOAD

Type	Hours	Percentage
Self study	90,0	60.00
Hours small group	15,0	10.00
Hours large group	45,0	30.00

Total learning time: 150 h

CONTENTS

1. Input/output

Description:
1.1. Devices I/O
1.2. Synchronizing I/O for Polling
1.3. Synchronizing I/O for Interruptions
1.3.B Exceptions
1.4. Direct Memory Access (DMA)

Related activities:
Activity 1: Problems Input / Output
Activity 2: Lab 1: synchronization by polling
Activity 3: Lab 2: synchronization by interruptions
Activity 4: Partial test of knowledge

Full-or-part-time: 42h
Theory classes: 15h
Laboratory classes: 6h
Self study : 21h

2. Cache Memory

Description:
2.1. Introduction to Memory Hierarchy
2.2. Cache memory
2.3. Impact of the Organization of memory cache performance
2.4. Performance Measures
2.5 Design Considerations and cache controller

Related activities:
Activity 1: Cache memory exercises
Activity 2: Lab 3: Memory cache

Full-or-part-time: 30h
Theory classes: 11h
Laboratory classes: 4h
Self study : 15h

3. Virtual Memory

Description:
3.1. Introduction
3.2. Address translation and pagination
3.3. Integrating virtual memory and cache

Related activities:
Activity 1: Virtual memory exercises

Full-or-part-time: 20h
Theory classes: 6h
Laboratory classes: 4h
Self study : 10h

4. Integration into an Operating System

Description:
In this chapter we will study in a very practical manner how the previously studied modules fit into an operating system.

Full-or-part-time: 28h
Theory classes: 10h
Self study : 18h

GRADING SYSTEM

Final Mark = (Partial test)*0,25 + (Lab)*0,30 + (Complementary work)*0,15 + (final test)*0,30 >=5
The final exam may be a partial exam with a weight of 30% or a final exam with a weight of 55% in order to recover the partial test (the best mark will be chosen). In this second case the formula is:
Laboratory * 0.30 + complementary work * 0.15 + Final test * 0.55> = 5
The final test can be reassessed.

BIBLIOGRAPHY

Basic:
- Patterson, David A. ; Hennessy, John L. Computer organization and design : the hardware/software interface. 6th ed. Oxford, GB: Morgan Kaufmann, 2021. ISBN 9780128201091.
- Patterson, David A; Hennessy, John L. Computer organization and design RISC-V edition : the hardware software interface. 2nd ed. Cambridge, MA: Morgan Kaufmann, 2021. ISBN 9780128203316.