Course guide
2301205 - SOC - Soc Design and Verification

Last modified: 29/05/2025

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 1022 - UAB - (ANG) pendent.

Degree: MASTER'S DEGREE IN SEMICONDUCTOR ENGINEERING AND MICROELECTRONIC DESIGN (Syllabus 2024). (Optional subject).

Academic year: 2025 **ECTS Credits:** 6.0 **Languages:** English

LECTURER

Coordinating lecturer: JORDI CARRABINA BORDOLL

Others: Primer quadrimestre:
JORDI CARRABINA BORDOLL - 11
MÀRIUS MONTÓN MACIAN - 11 + 9
OSCAR PALOMAR PÉREZ - 11 + 6

PRIOR SKILLS

Verilog HDL (Mandatori), C++ (Mandatori), HW/SW Codesign, Computer Architecture, FPGA Design, ASIC back-end, Process Design Kits (PDK), Electronic Design Automation (EDA) tools

LEARNING RESULTS

Knowledges:
KT01. Identify semiconductor devices, technological processes, the most appropriate microelectronic design tools, and relationships between these elements in order to integrate a given product or system into microelectronic technologies.
KT02. Describe the current state of scientific research and microelectronic industrial technology worldwide and their economic, social and environmental impact.
KT05. Describe the main methods and tools used to design integrated circuits and systems in accordance with the required functional specifications and cost of the final integrated product.
KT06. Identify and describe the main verification and test strategies for integrated circuits and systems according to their application.

Skills:
ST01. Design integrated devices, circuits and systems for new products according to their applications, taking into account sustainability and energy efficiency requirements.
ST02. Apply the manufacturing techniques and processes and design, simulation and characterisation tools of semiconductor engineering and microelectronic design to provide a solution to a specific integrated system proposal.

Competences:
CT01. Design new devices and integrated systems that require the use of manufacturing techniques specific to microelectronic technologies or the use of microelectronic design tools.
CT02. Apply sustainability criteria to projects based on integrated microelectronic products.
CT03. Apply the processes of semiconductor engineering and microelectronic design to fields in diverse areas of science or engineering where integrated systems are required.

TEACHING METHODOLOGY

Participatory Lectures. Resolution of exercises and problems. Laboratory practical work.

LEARNING OBJECTIVES OF THE SUBJECT

This course is centered in the design and verification of complex System-on-a-Chip (SoC) components in a meet-in-the middle platform-based design approach, that builds complex chips out of SoC modules starting from predefined components to be later synthesized on ASIC processes or FPGA devices for prototyping. System-level HW/SW co-design tools are used for both specification, synthesis and verification, reinforcing specially that one as a key aspect of the design flow.

STUDY LOAD

Type	Hours	Percentage
Self study	102,0	68.00
Hours large group	33,0	22.00
Hours small group	15,0	10.00

Total learning time: 150 h

CONTENTS

SoC Architectures

Description:
Elementary SoC architecture (HW+SW).
Selection of Implementation Technologies
SoC Design with Virtual Components (IPs).
On-chip-buses & related infrastructure (AMBA AXI OCB).
Memory types and Architecture.
Processor cores and ecosystems (ARM, RISC-V).
Real implementation Examples.

Related competencies :
CT02. Apply sustainability criteria to projects based on integrated microelectronic products.
CT03. Apply the processes of semiconductor engineering and microelectronic design to fields in diverse areas of science or engineering where integrated systems are required.
CT01. Design new devices and integrated systems that require the use of manufacturing techniques specific to microelectronic technologies or the use of microelectronic design tools.
KT02. Describe the current state of scientific research and microelectronic industrial technology worldwide and their economic, social and environmental impact.
KT05. Describe the main methods and tools used to design integrated circuits and systems in accordance with the required functional specifications and cost of the final integrated product.
KT01. Identify semiconductor devices, technological processes, the most appropriate microelectronic design tools, and relationships between these elements in order to integrate a given product or system into microelectronic technologies.
ST02. Apply the manufacturing techniques and processes and design, simulation and characterisation tools of semiconductor engineering and microelectronic design to provide a solution to a specific integrated system proposal.
ST01. Design integrated devices, circuits and systems for new products according to their applications, taking into account sustainability and energy efficiency requirements.

Full-or-part-time: 34h 22m
Theory classes: 11h
Self study : 23h 22m

Verification languages and methodologies

Description:
Verification concepts and methodologies. SystemVerilog for Verification. Simple and Complex testbenches. Correctness checking. Randomization and coverage (code and functional). Assertions.

Related competencies :
CT01. Design new devices and integrated systems that require the use of manufacturing techniques specific to microelectronic technologies or the use of microelectronic design tools.
KT05. Describe the main methods and tools used to design integrated circuits and systems in accordance with the required functional specifications and cost of the final integrated product.
KT01. Identify semiconductor devices, technological processes, the most appropriate microelectronic design tools, and relationships between these elements in order to integrate a given product or system into microelectronic technologies.
KT06. Identify and describe the main verification and test strategies for integrated circuits and systems according to their application.
ST02. Apply the manufacturing techniques and processes and design, simulation and characterisation tools of semiconductor engineering and microelectronic design to provide a solution to a specific integrated system proposal.

Full-or-part-time: 34h 23m
Theory classes: 11h
Self study : 23h 23m

High-level modelling languages and methodologies

Description:
SystemC TLM. Co-simulation SystemC–HDL. High-level synthesis tools.

Related competencies :
CT03. Apply the processes of semiconductor engineering and microelectronic design to fields in diverse areas of science or engineering where integrated systems are required.
CT01. Design new devices and integrated systems that require the use of manufacturing techniques specific to microelectronic technologies or the use of microelectronic design tools.
KT05. Describe the main methods and tools used to design integrated circuits and systems in accordance with the required functional specifications and cost of the final integrated product.
KT01. Identify semiconductor devices, technological processes, the most appropriate microelectronic design tools, and relationships between these elements in order to integrate a given product or system into microelectronic technologies.
KT06. Identify and describe the main verification and test strategies for integrated circuits and systems according to their application.
ST02. Apply the manufacturing techniques and processes and design, simulation and characterisation tools of semiconductor engineering and microelectronic design to provide a solution to a specific integrated system proposal.
ST01. Design integrated devices, circuits and systems for new products according to their applications, taking into account sustainability and energy efficiency requirements.

Full-or-part-time: 34h 23m
Theory classes: 11h
Self study : 23h 23m

Laboratory sessions

Description:
1. SoC architectural customization (AXI, MMAP, IRQs, DMA,...) with virtual components (IPs)
2. SystemVerilog SoC testbench on AXI
3. Assertions and coverage
4. SystemC TLM HW/SW co-simulation of the SoC (I)
5. SystemC TLM HW/SW co-simulation of the SoC (II)

Specific objectives:
Students work with virtual components (IPs), connected to an integrated bus (OCB). The design of a specific SoC begins with the selection of its components and building its architecture, continues with functional verification at the level of individual components or small groups with SystemVerilog, and ends with the HW/SW co-simulation of the complete SoC with SystemC TLM, prior to start back-end synthesis.

Related activities:
5 practical sessions of 3 hours each

Related competencies :
CT02. Apply sustainability criteria to projects based on integrated microelectronic products.
CT03. Apply the processes of semiconductor engineering and microelectronic design to fields in diverse areas of science or engineering where integrated systems are required.
CT01. Design new devices and integrated systems that require the use of manufacturing techniques specific to microelectronic technologies or the use of microelectronic design tools.
KT02. Describe the current state of scientific research and microelectronic industrial technology worldwide and their economic, social and environmental impact.
KT05. Describe the main methods and tools used to design integrated circuits and systems in accordance with the required functional specifications and cost of the final integrated product.
KT01. Identify semiconductor devices, technological processes, the most appropriate microelectronic design tools, and relationships between these elements in order to integrate a given product or system into microelectronic technologies.
KT06. Identify and describe the main verification and test strategies for integrated circuits and systems according to their application.
ST02. Apply the manufacturing techniques and processes and design, simulation and characterisation tools of semiconductor engineering and microelectronic design to provide a solution to a specific integrated system proposal.
ST01. Design integrated devices, circuits and systems for new products according to their applications, taking into account sustainability and energy efficiency requirements.

Full-or-part-time: 46h 40m
Laboratory classes: 15h
Self study : 31h 40m

GRADING SYSTEM

Individual assignments and activities (20%). Final exam (40%). Laboratory group work (40%, it is mandatory to pass it to pass the subject).

BIBLIOGRAPHY

Basic:
- Keating, M. The simple art of SoC design [on line]. New York, NY: Springer New York, 2011 [Consultation: 13/06/2024]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-1-4419-8586-6. ISBN 9781441985866.
- Patterson, D.; Waterman, A. The RISC-V reader: an open architecture atlas [on line]. San Francisco: Strawberry Canyon, 2017 [Consultation: 11/06/2024]. Available on: http://riscvbook.com/. ISBN 9780999249116.
- Spear, C.; Tumbush, G. SystemVerilog for verification: a guide to learning the testbench language features [on line]. 3rd ed. New York, NY: Springer, 2012 [Consultation: 11/06/2024]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-1-4614-0715-7. ISBN 9781461407157.
- Kogel, T.; Leupers, R. ; Meyr, H. Integrated system-level modeling of network-on-chip enabled multi-processor platforms [on line]. Dordrecht, The Netherlands: Springer, 2006 [Consultation: 13/06/2024]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/1-4020-4826-2. ISBN 9781402048258.

Complementary:
- Chakravarthi, V.S. A practical approach to VLSI system on chip (SoC) design: a comprehensive guide [on line]. 1st ed. 2020. Cham: Springer Cham, 2020 [Consultation: 11/06/2024]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-3-030-23049-4. ISBN 9783030230494.
- Flynn, M.J.; Luk, W. Computer system design: system-on-chip [on line]. Hoboken: Wiiey, 2011 [Consultation: 11/06/2024]. Available on: https://ebookcentral-proquest-com.recursos.biblioteca.upc.edu/lib/upcatalunya-ebooks/detail.action?pq-origsite=primo&docID=693260. ISBN 9781118009901.
- Greaves, D.J. Modern system-on-chip design on Arm. Cambridge: Arm Education Media, 2021. ISBN 9781911531364.
- Beuchat, R.; Depraz, F.; Guerrieri, A.; Kashani, S. Fundamentals of system-on-chip: design on Arm Cortex-M microcontrollers. Cambridge: Arm Education Media, 2021. ISBN 9781911531333.
- Mehta, A.B. ASIC/SoC functional design verification [on line]. Springer, 2017 [Consultation: 11/06/2024]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-3-319-59418-7. ISBN 9783319594187.
- Wile, B.; Goss, J.C.; Roesner, W. Comprehensive functional verification: the complete industry cycle [on line]. 1st ed. Amsterdam ; Boston: Elsevier/Morgan Kaufmann, 2005 [Consultation: 13/06/2024]. Available on: https://ebookcentral-proquest-com.recursos.biblioteca.upc.edu/lib/upcatalunya-ebooks/detail.action?pq-origsite=primo&docID=234976. ISBN 9780080476643.
- Taraate, V. Digital logic design using Verilog: coding and RTL synthesis [on line]. 2nd ed. Singapore: Springer, 2023 [Consultation: 13/06/2024]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-981-16-3199-3. ISBN 9789811946523.
- Herdt, V.; Drechsler, R.; Grosse, D. Enhanced virtual prototyping: featuring RISC-V case studies [on line]. Cham, Switzerland: Springer, 2021 [Consultation: 13/06/2024]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-3-030-54828-5. ISBN 9783030548285.

RESOURCES

Computer material:
- EDA tools: Siemens QuestaSIM (https://eda.sw.siemens.com/en-US/ic/questa-one/simulation/questa-one-sim/) Siemens Catapult HLS (https://eda.sw.siemens.com/en-US/ic/catapult-high-level-synthesis/). EDA tools

Other resources:
IPs: Open source RISC-V processors, peripherals and tools.
EDA tools for design and verification.