Course guide
2301206 - ICPD - Integrated Circuits Physical Design

Last modified: 29/05/2025

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: MASTER'S DEGREE IN SEMICONDUCTOR ENGINEERING AND MICROELECTRONIC DESIGN (Syllabus 2024). (Optional subject).

Academic year: 2025 **ECTS Credits:** 6.0 **Languages:** English

LECTURER

Coordinating lecturer: Canals Gil, Joan

Others: Primer quadrimestre:
RAIMON CASANOVA MOHR - 11
JOAN CANALS GIL - 11
FRANCESC DE BORJA MOLL ECHETO - 11

PRIOR SKILLS

Digital design
Contents of the course Microelectronic Design (MD)

LEARNING RESULTS

Knowledges:
KT01. Identify semiconductor devices, technological processes, the most appropriate microelectronic design tools, and relationships between these elements in order to integrate a given product or system into microelectronic technologies.
KT03. Describe the physical principles underlying current semiconductor devices in relation to their application, as well as their emerging trends, modelling and characterisation techniques.
KT04. Identify and describe the different manufacturing and characterisation processes in microelectronics and their applicability according to the functional and cost requirements of the final integrated product.
KT05. Describe the main methods and tools used to design integrated circuits and systems in accordance with the required functional specifications and cost of the final integrated product.
KT06. Identify and describe the main verification and test strategies for integrated circuits and systems according to their application.

Skills:
ST01. Design integrated devices, circuits and systems for new products according to their applications, taking into account sustainability and energy efficiency requirements.
ST02. Apply the manufacturing techniques and processes and design, simulation and characterisation tools of semiconductor engineering and microelectronic design to provide a solution to a specific integrated system proposal.

Competences:
CT01. Design new devices and integrated systems that require the use of manufacturing techniques specific to microelectronic technologies or the use of microelectronic design tools.
CT02. Apply sustainability criteria to projects based on integrated microelectronic products.
CT03. Apply the processes of semiconductor engineering and microelectronic design to fields in diverse areas of science or engineering where integrated systems are required.

TEACHING METHODOLOGY

Presentation by the professor (master class)
Laboratory work with EDA design tools

LEARNING OBJECTIVES OF THE SUBJECT

Knowledge:
K1.1 Apply the methodologies and tools for the design and verification of semicustom digital integrated circuits.
K.1.2 Understand the advantages and limitations of digital microelectronic technologies and the characteristics of design kits (PDKs).
K.1.3 Understand the restrictions, temporal aspects and energy consumption in a design.
K1.4 Develop appropriate test strategies for digital integrated circuits.
Skills:
S1.1 Design digital integrated circuits using automatic logical and physical synthesis tools according to specifications.
S1.2 Use verification tools at a logical and physical level.
S1.3 Use design tools to test integrated circuits.
Competencies:
C1.1 Make digital integrated circuits with efficiency in terms of area, consumption, speed and testability.

STUDY LOAD

Type	Hours	Percentage
Hours small group	24,0	16.00
Self study	102,0	68.00
Hours large group	24,0	16.00

Total learning time: 150 h

CONTENTS

T0. Concepts and methodology.

Description:
Implementation styles. Digital design flow. Tools for automatic design.

Full-or-part-time: 1h
Theory classes: 1h

T1. Hardware Description Languages (HDL): Systemverilog

Description:
Systemverilog review. Modeling of digital systems for synthesis. Use of HDLs for simulation/verification.

Full-or-part-time: 4h
Theory classes: 4h

T2. Synthesis and implementation of digital integrated circuits

Description:
Stages of the synthesis process. Libraries. Optimizations in the functional and logical synthesis process. Constraints of a design (SDC). Temporal analysis - Static Timing Analysis (STA). Physical synthesis: Floorplan, Placement, Clock-Tree synthesis (CTS), Routing, Timing optimization and GDS generation.

Full-or-part-time: 9h
Theory classes: 9h

T3. Physical verification

Description:
RTL Linting. Synchronization and CDC checks. Timing closure. Power modeling. Power distribution analysis.

Full-or-part-time: 2h
Theory classes: 2h

T4. Advanced physical implementation

Description:
Low power techniques. UPF modeling and flow.

Full-or-part-time: 3h
Theory classes: 3h

T5. Design for testability

Description:
Test concepts. Failure models. Test generation in combinational and sequential circuits. IDDQ. Automatic vector generation methods. Design for testing. Scan chains. Boundary scan. Built-in self-test.

Full-or-part-time: 7h
Theory classes: 7h

L1. Digital simulation

Description:
Simulation of a design in RTL. Gate level simulation.

Full-or-part-time: 4h
Laboratory classes: 4h

L2. Logic synthesis (6h)

Description:
Logical synthesis of a moderately complex design

Full-or-part-time: 6h
Laboratory classes: 6h

L3. Static timing analysis. Physical verification

Description:
Timing analysis and effect of timing constraints. Power check. Layout verification.

Full-or-part-time: 4h
Laboratory classes: 4h

L4. Full flow: logic equivalence check, CDC check, implementation (4h)

Description:
Design implementation with multiple clock domains. Advanced checks.

Full-or-part-time: 4h
Laboratory classes: 4h

L5. DFT: ATPG, scan insertion, BIST

Description:
Design flow for testability. Synthesis and physical implementation.

Full-or-part-time: 4h
Laboratory classes: 4h

GRADING SYSTEM

Partial and final exams (50% overall)
Delivery of laboratory reports (50%)

BIBLIOGRAPHY

Basic:

- Bhasker, J; Chadha, R. Static timing analysis for nanometer designs: a practical approach [on line]. New York: Springer, 2009 [Consultation: 13/06/2024]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-0-387-93820-2. ISBN 9780387938196.
- Mehta, A.B. Introduction to SystemVerilog [on line]. Cham, Switzerland: Springer, 2021 [Consultation: 13/06/2024]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-3-030-71319-5. ISBN 9783030713195.
- Golshan, K. Physical design essentials: an ASIC design implementation perspective [on line]. New York: Springer, 2007 [Consultation: 13/06/2024]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-0-387-46115-1. ISBN 9780387461151.