Course guide
2301207 - AICD - Analog Ic Design

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Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 1022 - UAB - (ANG) pendent.

Degree: MASTER'S DEGREE IN SEMICONDUCTOR ENGINEERING AND MICROELECTRONIC DESIGN (Syllabus 2024). (Optional subject).

Academic year: 2025 **ECTS Credits:** 6.0 **Languages:** English

LECTURER

Coordinating lecturer: FRANCESC SERRA GRAELLS

Others: Primer quadrimestre:
RAIMON CASANOVA MOHR - 11
DAVID GASCON FORA - 11
PEDRO LUÍS MIRIBEL CATALÀ - 11
JORDI SACRISTÁN RIQUELME - 11
FRANCESC SERRA GRAELLS - 11

LEARNING RESULTS

Knowledges:
KT01. Identify semiconductor devices, technological processes, the most appropriate microelectronic design tools, and relationships between these elements in order to integrate a given product or system into microelectronic technologies.
KT02. Describe the current state of scientific research and microelectronic industrial technology worldwide and their economic, social and environmental impact.
KT05. Describe the main methods and tools used to design integrated circuits and systems in accordance with the required functional specifications and cost of the final integrated product.
KT06. Identify and describe the main verification and test strategies for integrated circuits and systems according to their application.

Skills:
ST01. Design integrated devices, circuits and systems for new products according to their applications, taking into account sustainability and energy efficiency requirements.
ST02. Apply the manufacturing techniques and processes and design, simulation and characterisation tools of semiconductor engineering and microelectronic design to provide a solution to a specific integrated system proposal.

Competences:
CT01. Design new devices and integrated systems that require the use of manufacturing techniques specific to microelectronic technologies or the use of microelectronic design tools.
CT02. Apply sustainability criteria to projects based on integrated microelectronic products.
CT03. Apply the processes of semiconductor engineering and microelectronic design to fields in diverse areas of science or engineering where integrated systems are required.

TEACHING METHODOLOGY

Teaching methodology is based on classroom lectures and exercises (32h) and lab sessions (16h). The lab work includes the full-custom design of a two-stage Miller Opamp from functional specifications to full-custom layout in CMOS technology with industrial electronic design automation (EDA) tools and process design kit (PDK).

LEARNING OBJECTIVES OF THE SUBJECT

This course is an introduction to the specific full-custom design techniques of analog integrated circuits in CMOS technologies. Besides the required knowledge at process, device and circuit levels, it provides hands on practice of the full-custom schematic and physical design methodologies to develop analog application-specific integrated circuits (ASICs) projects from specifications to tapeout.

Specific objectives:

1. Acquire knowledge on specific full-custom analog design techniques for integrated circuits at research and industrial levels with emphasis on low-power and low-noise scenarios.
2. Be able to select the most suitable CMOS technology given a set of specifications for an application-specific integrated circuit (ASIC) design project.
3. Learn to assess the different steps involved in the full-custom analog design methodology of integrated circuits both at schematic and layout levels.
4. Acquire hands on practice of industrial full-custom electronic design automatic (EDA) tools and CMOS process design kits (PDKs).

STUDY LOAD

Type	Hours	Percentage
Self study	102,0	68.00
Hours large group	32,0	21.33
Hours small group	16,0	10.67

Total learning time: 150 h

CONTENTS

Introduction to Full-Custom Analog ICs

Description:
More than Moore versus More Moore. IC design flavors: from full-custom application-specific integrated circuits (ASICs) to third-party IP libraries. Mixed-signal CMOS technology modules. ASIC prototyping strategies (MPW, MLM, stitching). Impact of CMOS technology size and supply voltage downscaling in analog circuits. Trending topics and challenges in analog IC design.

Full-or-part-time: 2h
Theory classes: 2h

Device Modeling for Analog CMOS Design

Description:
Transistor modeling suitable for analog hand design. MOSFET EKV model (I/V, transconductance, capacitance, noise). Subthreshold operation and circuit design driven by inversion coefficient (IC). BJTs and passive devices (planar resistors, MiM and MoM capacitors). Device process corners and technology mismatching.

Full-or-part-time: 4h
Theory classes: 4h

CMOS Operational Amplifiers

Description:
Black-box figures of merit (gain, GBW, settling time, SR, offset, equivalent input noise, CMR, CMRR, PSRR). OpAmp building blocks at transistor level (common-S/G and back-gate stages, current mirrors, buffers, level shifters). Differential OpAmps and common-mode feedback (CMFB). Cascoding and gain boosting techniques. Folded and telescopic topologies. Stability and frequency compensation in multi-stage OpAmps.

Full-or-part-time: 6h
Theory classes: 6h

Full-Custom Analog IC Design Methodology

Description:
Schematic and physical design flows. Full-custom electronic design automation (EDA) tools and CMOS process design kit (PDK). Guidelines for analog device sizing. Simulation analysis of analog circuits: large-signal DC, small-signal AC, transient, noise, sensitivity, periodic steady-state (PSS). The art of analog layout for signal decoupling and device matching. Parametrized cells (PCells). Physical verification (DRC, LVS, PEX) and post-layout simulation. Design for manufacturing (DFM).

Full-or-part-time: 4h
Theory classes: 4h

Low-Power Operational Amplifiers

Description:
Low-power IC scenarios (battery supply, remote power, energy harvesting). Low-current versus low-voltage OpAmps. Subthreshold operation. Dynamic biasing. Class-AB output stages. Rail-to-rail topologies. Inverter-based pseudo-differential amplifiers.

Full-or-part-time: 4h
Theory classes: 4h

Low-Noise Circuit Techniques

Description:
OpAmp noise optimization in low-frequency sensing applications. Chopping circuit topologies. Correlated double sampling (CDS) techniques.

Full-or-part-time: 4h
Theory classes: 4h

Specific Building Blocks

Description:
Analog voltage references and bias current generators (PTAT, bandgap). Comparators. Current-mode circuits (conveyors, splitters, WTA). Linear transconductors and GmC filters. Switched-capacitor circuits (S/H, T/H, amplifiers, filters). Oscillators.

Full-or-part-time: 8h
Theory classes: 8h

GRADING SYSTEM

Evaluation according to the following weighted rule: proposed exercises (10%), lab report (40%) and exam (50%). If exam mark is under 4/10, a remedial exam needs to be passed and its mark is downscaled to 80%.

BIBLIOGRAPHY

Basic:
- Allen, P.E.; Holberg, D.R. CMOS analog circuit design. New York: Oxford University Press, 2012. ISBN 9780199937424.
- Razavi, B. Design of analog CMOS integrated circuits. 2nd ed. Boston: McGraw Hill, 2017. ISBN 9781259255090.
- Gray, P.R.; Hurst, P.J.; Lewis, S.H. Analysis and design of analog integrated circuits. 6th ed. Hoboken, New Jersey: Wiley, 2024. ISBN 9781394220069.
- Sansen, W.M. Analog design essentials [on line]. New York, NY: Springer US, 2006 [Consultation: 27/06/2024]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/b135984. ISBN 9780387257471.
- Hastings, A. The art of analog layout. 2nd ed. Upper Saddle River: Prentice Hall, 2006. ISBN 9780131464100.