

Course guide

2301218 - MSIPD - Mixed Signal IP Design

Last modified: 29/05/2025

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 1022 - UAB - (ANG) pendent.

Degree: MASTER'S DEGREE IN SEMICONDUCTOR ENGINEERING AND MICROELECTRONIC DESIGN (Syllabus 2024).
(Optional subject).

Academic year: 2025 **ECTS Credits:** 4.0 **Languages:** English

LECTURER

Coordinating lecturer: FRANCESC SERRA GRAELLS

Others: Segon quadrimestre:
RAIMON CASANOVA MOHR - 11
DAVID GASCON FORA - 11
JORDI SACRISTÁN RIQUELME - 11
FRANCESC SERRA GRAELLS - 11

LEARNING RESULTS

Knowledges:

- KT01. Identify semiconductor devices, technological processes, the most appropriate microelectronic design tools, and relationships between these elements in order to integrate a given product or system into microelectronic technologies.
- KT02. Describe the current state of scientific research and microelectronic industrial technology worldwide and their economic, social and environmental impact.
- KT03. Describe the physical principles underlying current semiconductor devices in relation to their application, as well as their emerging trends, modelling and characterisation techniques.
- KT04. Identify and describe the different manufacturing and characterisation processes in microelectronics and their applicability according to the functional and cost requirements of the final integrated product.
- KT05. Describe the main methods and tools used to design integrated circuits and systems in accordance with the required functional specifications and cost of the final integrated product.
- KT06. Identify and describe the main verification and test strategies for integrated circuits and systems according to their application.

Skills:

- ST01. Design integrated devices, circuits and systems for new products according to their applications, taking into account sustainability and energy efficiency requirements.
- ST02. Apply the manufacturing techniques and processes and design, simulation and characterisation tools of semiconductor engineering and microelectronic design to provide a solution to a specific integrated system proposal.

Competences:

- CT01. Design new devices and integrated systems that require the use of manufacturing techniques specific to microelectronic technologies or the use of microelectronic design tools.
- CT02. Apply sustainability criteria to projects based on integrated microelectronic products.
- CT03. Apply the processes of semiconductor engineering and microelectronic design to fields in diverse areas of science or engineering where integrated systems are required.

TEACHING METHODOLOGY

Teaching methodology is based on classroom lectures and exercises (20h) and lab sessions (10h). The lab work includes the top-down design of a switched-capacitor (SC) Delta-Sigma ADC or clock PLL IP block from functional specifications to layout in CMOS technology with electronic design automation (EDA) tools and process design kit (PDK).

LEARNING OBJECTIVES OF THE SUBJECT

This course is an introduction to the CMOS design of mixed-signal IP blocks, from the functional specification employing Verilog-A description language to the physical integration in big-A and big-D systems on chip (SoCs). The top-down mixed-signal design methodology is applied to three key families of IP blocks: A/D and D/A data converters and clock phase-locked loops (PLLs). The course also provides hands on practice of the optimization of these mixed-signal IP blocks using electronic design automatic (EDA) tools and CMOS process design kits (PDKs).

Specific objectives:

1. Learn to assess the different steps involved in the top-down design methodology of mixed-signal IP blocks in CMOS technologies for systems on chip (SoCs).
2. Be able to specify a mixed-signal IP block using Verilog-A hardware description language (HDL).
3. Acquire knowledge on specific design techniques for three families of mixed-signal IP blocks: A/D and D/A data converters and clock phase-locked loops (PLLs).
4. Acquire hands on practice of mixed-signal IP optimization employing both open and industrial electronic design automatic (EDA) tools and CMOS process design kits (PDKs).

STUDY LOAD

Type	Hours	Percentage
Hours large group	20,0	20.00
Self study	70,0	70.00
Hours small group	10,0	10.00

Total learning time: 100 h

CONTENTS

Introduction to Mixed-Signal CMOS Design Flows

Description:

Top-down design methodology of mixed-signal ICs. IP block specification through IC architecture functional simulation. IP block integration in big-A and big-D IC design flows. Best practices for IP portability in CMOS technologies. Trending topics and challenges in mixed-signal IP circuit design.

Full-or-part-time: 1h

Theory classes: 1h

IP Architecture Modeling with Verilog-A

Description:

Mixed-signal circuit simulation techniques: electrical network versus event driven. Analog hardware description languages (AHDLS). Introduction to Verilog-A language: basics (data types, expressions, signals, functions), analog behavior and design hierarchy.

Full-or-part-time: 3h

Theory classes: 3h

Analog-to-Digital Data Converters

Description:

Sampling and quantization in data conversion. ADC figures of merit (DNL, INL, SNDR, ENOB, DR, OSR, FOMS/W). Flash ADCs. Sub-ranging, time-interleaving and pipelining. Successive-approximation (SAR) A/D converters. Oversampled Delta-Sigma modulators (CT, SC, DEM, IADC, Zoom). Asynchronous integrate-and-fire (IAF) modulators. Time-domain conversion (TDC).

Full-or-part-time: 6h

Theory classes: 6h

Digital-to-Analog Data Converters

Description:

Multi-stage noise shaping (MASH) D/A converters. Pulse modulation techniques.

Full-or-part-time: 2h

Theory classes: 2h

Integer-N Clock Phase-Locked Loops

Description:

Basic PLL architecture. Controlled oscillators and frequency dividers. Phase/frequency detectors and charge pumps. Loop filter and PLL stability. Phase noise, jitter and lock-in time figures of merit.

Full-or-part-time: 4h

Theory classes: 4h

Automatic Circuit Optimization

Description:

Analysis of IP performance versus resources (power and area). IP circuit parametrization for optimization. General optimization rules and algorithms. Multi-variable cost functions. Optimization against CMOS process, supply voltage and temperature range (PVT).

Full-or-part-time: 2h

Theory classes: 2h

Mixed-Signal EDA Tools

Description:

Open source and commercial electronic design automation (EDA) tools and CMOS process design kits (PDKs) for mixed-signal IP design. Mixed-signal circuit simulation and optimization tools.

Full-or-part-time: 2h

Theory classes: 2h

GRADING SYSTEM

Evaluation according to the following weighted rule: proposed exercises (10%), lab report (40%) and exam (50%). If exam mark is under 4/10, a remedial exam needs to be passed and its mark is downscaled to 80%.

BIBLIOGRAPHY

Basic:

- Plassche, R. van de. CMOS integrated analog-to-digital and digital-to-analog converters. 2nd ed. Boston [etc.]: Kluwer Academic, 2003. ISBN 9781402075001.
- Pavan, S.; Schreier, R.; Temes, G.C. Understanding delta-sigma data converters [on line]. 2nd ed. Hoboken, New Jersey: John Wiley & Sons, Inc. : IEEE Press, 2017 [Consultation: 16/07/2024]. Available on: <https://onlinelibrary-wiley-com.recursos.biblioteca.upc.edu/doi/book/10.1002/9781119258308>. ISBN 9781119258308.
- Razavi, B. Design of CMOS phase-locked loops: from circuit level to architecture level. New York, NY: Cambridge University Press, 2020. ISBN 9781108494540.
- Accellera Systems Initiative. Verilog-AMS Language Reference Manual v2.4.0 [on line]. v2.4.0. Napa, CA: Accellera Systems Initiative Inc., 2014 [Consultation: 18/06/2024]. Available on: <https://www.accellera.org/images/downloads/standards/v-ams/VAMS-LRM-2-4.pdf>.
- Hastings, A. The art of analog layout. 2nd ed. Upper Saddle River: Prentice Hall, 2006. ISBN 9780131464100.