

Course guide

230660 - PROEL - Programmable Electronics

Last modified: 02/06/2022

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2013). (Optional subject).
MASTER'S DEGREE IN TELECOMMUNICATIONS ENGINEERING (Syllabus 2013). (Optional subject).
MASTER'S DEGREE IN ADVANCED TELECOMMUNICATION TECHNOLOGIES (Syllabus 2019). (Optional subject).

Academic year: 2022 **ECTS Credits:** 5.0 **Languages:** English

LECTURER

Coordinating lecturer: JOAN PONS

Others: JUAN ANTONIO CHÁVEZ, MARCO ANTONIO AZPURUA

PRIOR SKILLS

Fundamentals of digital electronics: number systems, binary codes, Boolean Algebra, analysis and design of combinational logic circuits, combinational modules, analysis and design of simple sequential circuits, sequential modules (registers, counters, etc.)
Fundamentals of CMOS technology.

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Transversal:

1. TEAMWORK: Being able to work in an interdisciplinary team, whether as a member or as a leader, with the aim of contributing to projects pragmatically and responsibly and making commitments in view of the resources that are available.
2. EFFECTIVE USE OF INFORMATION RESOURCES: Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.
3. FOREIGN LANGUAGE: Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

TEACHING METHODOLOGY

- Lectures
- Laboratory classes
- Personal work (distance)
- Short answer tests (midterm exams)
- Extended answer test (Final Exam)

LEARNING OBJECTIVES OF THE SUBJECT

Learning objectives of the subject:

The aim of this course is the presentation and use of advanced digital design tools and methodologies, with especial emphasis on hardware description languages, programmable logic devices and advanced design techniques for mid-complexity digital subsystems.

Learning results of the subject:

- Ability to design, implement and evaluate mid-complexity digital circuits, using programmable logic devices such as FPGAs and CPLDs.
- Ability to describe and evaluate logic circuits of medium complexity using the VHDL description language and associated tools.
- Knowledge of the features and characteristics of commercial programmable logic devices, such as CPLDs and FPGAs. Ability to understand the information provided by the manufacturers.
- Identification and modelling of mid-complex digital systems. Analysis and qualitative approaches, setting methods to validate the results.

STUDY LOAD

Type	Hours	Percentage
Hours large group	13,0	10.40
Self study	86,0	68.80
Hours small group	26,0	20.80

Total learning time: 125 h

CONTENTS

1. Introduction to modern digital design

Description:

- Digital electronic systems, structural & behavioural description, digital ICs and technology alternatives, CAD/CAE tools, design flow.
- Programmable logic devices: technologies, performance, mid-complexity (CPLDs, FPGAs) and modern architectures (SoPC).
- VHDL description language: basic components, libraries, concurrent and sequential structures, application examples.

Full-or-part-time: 39h

Theory classes: 3h

Laboratory classes: 10h

Self study : 26h

2. Algorithmic state machines

Description:

- Specification & design of finite state machines (FSMs). FSM concurrency.
- Algorithms and specification of algorithmic state machines (ASMs). Register transfer level description.
- ASM data subsystem: components and design.
- ASM specific control subsystem design and micro programmed control.

Full-or-part-time: 43h

Theory classes: 5h

Laboratory classes: 8h

Self study : 30h

3. Advanced design techniques and topics

Description:

- Power consumption & power estimation.
- Metastability.
- The synchronous / asynchronous interface.
- Time performance estimation.
- Clock and reset signal managing.

Full-or-part-time: 43h

Theory classes: 5h

Laboratory classes: 8h

Self study : 30h

ACTIVITIES

(CAT) LABORATORY

Description:

- Module 1: Introduction to the design software & hardware tools (8h).
- Module 2: VHDL hierarchical design (9h).
- Module 3: ASM design (9h).

Full-or-part-time: 26h

Laboratory classes: 26h

HOMEWORK

Description:

Realization and delivery of 3 or 4 small works, exercises, etc. to do individually at home.

Full-or-part-time: 6h

Self study: 6h

SHORT ANSWER TESTS (CONTROL)

Description:

Two short exams to be done during the course.

Full-or-part-time: 2h

Theory classes: 2h

EXTENDED ANSWER TEST (FINAL EXAMINATION)

Description:

Final examination.

Full-or-part-time: 3h

Theory classes: 3h



GRADING SYSTEM

Final Score: 60% from Theory grade + 40% from Laboratory grade

The Theory grade is the maximum between ...

- 100% from Final examination,
- 50% from Final examination + 50% from partial examinations, controls and other activities done during the course.

It is possible to get rid of the Final examination if the grade of the partial exams and other works carried out during the course (called CTG) is 7.5 or more. In that case, the CTG becomes the Theory grade.

EXAMINATION RULES.

During the exams it is not allowed to use wireless devices (mobile phones, laptops, tablets, etc..) nor programmable calculators. It is also necessary to provide some identification document (ID card, passport, etc.)

BIBLIOGRAPHY

Basic:

- Balch, M. Complete digital design: a comprehensive guide to digital electronics and computer system architecture. New York: McGraw-Hill, 2003. ISBN 978-0071737708.
- Zwolinski, M. Digital system design with VHDL. 2nd ed. Harlow, England: Prentice-Hall, 2004. ISBN 013039985X.

Complementary:

- Rushton, A. VHDL for logic synthesis [on line]. 3rd ed. Wiley, 2011 [Consultation: 21/06/2017]. Available on: <http://onlinelibrary.wiley.com/book/10.1002/9781119995852>. ISBN 9781119995852.
- Lee, S. Advanced digital logic design: using VHDL, state machines, and synthesis for FPGAs. Southbank: Thomson, 2006. ISBN 978-0534466022.