Course guide
230667 - SCPD - System on Chip Physical Design

Last modified: 25/05/2023

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2013). (Optional subject).
MASTER'S DEGREE IN ADVANCED TELECOMMUNICATION TECHNOLOGIES (Syllabus 2019). (Optional subject).
MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2022). (Optional subject).

Academic year: 2023 **ECTS Credits:** 5.0 **Languages:** English

LECTURER

Coordinating lecturer: Consultar aquí / See here: https://telecos.upc.edu/ca/estudis/curs-actual/professorat-responsables-coordinadors/responsables-assignatura

Others: Consultar aquí / See here: https://telecos.upc.edu/ca/estudis/curs-actual/professorat-responsables-coordinadors/professorat-assignat-idioma

PRIOR SKILLS

Having concluded and passed the subject Digital Nanoelectronic Design (DND)
Knowledge of CMOS technology and design.
Knowledge of digital design, combinational and sequential.
Knowledge of standard cell design flow: synthesis and place and route.
Knowledge of Static Timing Analysis,
Previous experience with EDA tools for synthesis (Genus or DC) and place and route (Innovus or ICC2)

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
CEE18. Ability to design CMOS digital and analog integrated circuits of medium complexity.
CEE19. Ability to apply low-power techniques to integrated circuits (ICs).

Transversal:
1. TEAMWORK: Being able to work in an interdisciplinary team, whether as a member or as a leader, with the aim of contributing to projects pragmatically and responsibly and making commitments in view of the resources that are available.

2. EFFECTIVE USE OF INFORMATION RESOURCES: Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.

3. FOREIGN LANGUAGE: Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

TEACHING METHODOLOGY

- Lectures
- Laboratory activities
- Individual work
- Research topic presentation, individual or groups of two people
- Short answer test and exercises

LEARNING OBJECTIVES OF THE SUBJECT

Learning objectives of the subject:

The aim of this course is to train students in methods of design of digital CMOS integrated circuits from a high level description to a layout in an efficient way using computers so that the resulting layout satisfies topological, geometric, timing and power-consumption constraints of the design.

Learning results of the subject:

- Ability to understand and apply timing and power constraints to a complex integrated circuit.
- Ability to perform the physical implementation of a complex integrated circuit.
- Ability to apply low power design techniques to integrated circuit design.
- Ability to develop techniques for the design, analysis and evaluation of electronic systems in applications such as automation, aerospace, energy distribution and generation, consumer electronics, biomedicine, etc.
- Ability to analyze, design and evaluate microelectronic integrated circuits.
- Ability to implement advanced design techniques of microelectronic integrated circuits.
- Ability to use state of the art computer aided design (CAD) tools for the design of integrated circuits.

STUDY LOAD

Type	Hours	Percentage
Hours large group	13,0	10.40
Hours small group	26,0	20.80
Self study	86,0	68.80

Total learning time: 125 h

CONTENTS

Introduction to VLSI design, Technology evolution and state of the art.

Description:
Basis of modern integrated circuits (IC) design and technology. Moore's Law. Evolution of microprocessors and memories during the last decades. Key technology changes in the IC progress. Bulk and 3D technologies, other alternatives. State of the art and foreseen evolution.

Full-or-part-time: 3h
Theory classes: 1h
Self study : 2h

Design challenges. Computer Aided Design Tools. Design flow.

Description:
Evolution of design complexity in comparison with technology evolution. Design steps, design flow. High level description and synthesis. Hardware description languages, RTL level, architecture level, gate level. Verilog and VHDL languages. Placement and routing. Physical level requirements. Tools for verification and test.

Full-or-part-time: 3h
Theory classes: 1h
Self study : 2h

Digital CMOS circuits delay models. Voltage scaling impact. Pipeline. Timing violations.

Description:
Basic RC delay model for CMOS digital circuits. Advanced delay models in Spice simulator. Parasitic capacitances in layout, interconnection modeling. Analytical delay model, impact of voltage scaling in logic circuits. Timing requirements in sequential circuits, performances. Timing violation concept. Pipeline architectures.

Full-or-part-time: 3h
Theory classes: 1h
Self study : 2h

Digital CMOS circuits power components and models. Dynamic and Static power components models. Voltage and frequency scaling.

Description:
Power consumption evolution of modern integrated circuits. Power dissipation limits. Packaging, limit temperatures. Mechanisms of power dissipation in CMOS digital circuits. Static components, power dissipation due to subthreshold currents, models. Dynamic components, switching capacitance dissipation, model. Effect of voltage and frequency scaling.

Full-or-part-time: 3h
Theory classes: 1h
Self study : 2h

Low Power Design techniques.

Description:
Gate, Data and Power scaling. Impact of modern design strategies for low power design, examples of modern integrated circuits. Principles of clock gating, data gating and voltage and frequency scaling.
Multiple threshold voltage, multiple voltage islands, body bias modulation in FDSOI technology. Optimization of integrated circuit design using multiple threshold voltages strategy. Impact on power and performances. Multiple islands techniques, concept of level shifter cells. Substrate biasing concept, application in FDSOI technology.

Full-or-part-time: 6h
Theory classes: 2h
Self study : 4h

Thermal power models. Impact on delay and power. Self-heating.

Description:
Concept of power dissipation chain, models, parameter calculation, state of the art. Impact of power dissipation in the integrated circuit temperature. Static and dynamic evolution. Self-heating concept.

Full-or-part-time: 3h
Laboratory classes: 1h
Self study : 2h

Technology Scaling impact. Logic circuitry and interconnection models.

Description:
Scaling, the key factor of the integrated circuits progress. Moore's law and scaling. Limits in the photolithographic processes, evolution, state of the art and future prediction. Scaling models for circuitry and interconnections.

Full-or-part-time: 3h
Theory classes: 1h
Self study : 2h

IR and LdI/dt Vdd drops. Switching noise. Compensation techniques.

Description:
Dynamic current signals in digital switching circuits. Distribution of power supply wires, rings. Electrical models and voltage fluctuations due to dynamic and static voltage drops caused by parasitic capacitances. Decoupling capacitance techniques.

Full-or-part-time: 3h
Theory classes: 1h
Self study : 2h

Crosstalk between interconnections. Reliability issues.

Description:
Crosstalk coupling between parallel interconnection buses. Impact on delay and power. Models, evolution. Noise coupling through substrate and electromagnetic interferences. Concept of aging in MOS devices, hot carrier injection (HCI) and bias temperature instability (BTI) mechanism, impact, recovering mechanisms. Impact on reliability.

Full-or-part-time: 3h
Theory classes: 1h
Self study : 2h

Test of digital integrated circuits

Description:
Defects in manufacturing process. Test principles and objectives in the design integrated design and manufacturing. Fault models. Test techniques. Standards related with test, Scan Path and Boundary Scan path techniques.

Full-or-part-time: 3h
Theory classes: 1h
Self study : 2h

Alternative design techniques and technologies (emerging devices, neural networks)

Description:
Concept of memristor, characteristics. State of the art of memristive memories and processors. Concept of Computing In Memory. Memristive devices, ReRAM and STT-devices.
Concept of Neural Networks, memristors as synaptic units. Examples of neural network implementations.

Full-or-part-time: 3h
Theory classes: 1h
Self study : 2h

Laboratory: physical implementation of digital IC

Description:
Lab 1 Synthesis with physical information
Lab 2 Floorplanning a complete chip
Lab 3 Place and route
Lab 4 Full Flow: RTL to Place and Route with low power techniques

Full-or-part-time: 83h
Laboratory classes: 57h
Self study : 26h

Research topic presentation

Description:
The professors will propose a current topic related to digital design and technology. Each student or groups of two will do some research with current bibliography and present the state of the art on that topic to the rest of the class.

Full-or-part-time: 6h
Theory classes: 1h
Self study : 5h

GRADING SYSTEM

Continuous evaluation (CE):
- Two Partial exams: 16.6% each
- Research topic presentation: 16.6%
- Laboratory experiences: 50%

Final Exam (FE)

Final score: maximum (CE, FE)

EXAMINATION RULES.

Final exam: individual
Partial exams: individual
Research presentation: groups of up to two students
Laboratory: groups of up to two students

BIBLIOGRAPHY

Basic:
- Bhasker, J; Chadha, R.. Static timing analysis for nanometer designs, a practical approach [on line]. Boston, MA: Springer, 2009 [Consultation: 09/06/2021]. Available on: http://dx.doi.org/10.1007/978-0-387-93820-2. ISBN 9780387938202.
- Wang, L.T.; Chang, Y.W.; Ting, K. (eds.). Electronic design automation: synthesis, verification, and test. Burlington, MA: Morgan Kaufmann Publishers/Elsevier, 2009. ISBN 9780123743640.

RESOURCES

Other resources:
Slides of the course