Course guide
240IEE21 - 240IEE21 - Design on Silicon

Last modified: 13/03/2025

Unit in charge: Barcelona School of Industrial Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: MASTER'S DEGREE IN INDUSTRIAL ENGINEERING (Syllabus 2014). (Optional subject).

Academic year: 2025 **ECTS Credits:** 4.5 **Languages:** Catalan

LECTURER

Coordinating lecturer: SALVADOR MANICH BOU

Others: Salvador Manich Bou
Rosa Rodríguez Montañés
Álvaro Gómez Pau

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
CEEELECT1. Design electronic systems (mixed analogical and digital systems and micro-mechanical systems on silicon, digital systems based on discrete components, logical programable devices and/or microprocessors, electronic instrumentation systems and power electronic systems) and manage development projects and/or commercialization of electronic systems or development projects and/or commercialization of systems in which the electronic subsystems have an important specific weight.

TEACHING METHODOLOGY

The subject is assigned a teaching load of 4.5 ECTS credits, which is equivalent to a student dedication of 112.5 hours. 40 of these 112.5 hours correspond to face-to-face activities (24 hours of attendance to theory and problem classes, 10 hours of attendance to laboratory practices and 6 hours for evaluations). The other 72 hours correspond to non - contact activities (10 hours for the realization of simulations of circuits and systems of preparation of the practices and 62 hours of study.
The subject has been structured in two parts: a theoretical part and a practical part. Each of these parts involves face-to-face activities, directed non-face-to-face activities and evaluation activities.
The theoretical part includes the exposition of topics, the resolution and discussion of problems and examples, passing from one activity to another at the discretion of the teacher. The program indicated in the contents will be followed. The face-to-face activities of the theoretical part will consist of classes that will take place throughout the weeks of the academic year, in the groups and schedules established for this purpose by Ordinance of Studies, totaling a minimum of 24 hours of class (16 sessions of 1.5 hours each).
The practical part includes the realization of a project that will involve a set of circuits that must be simulated and/or experienced. The face-to-face activities of the practical part will consist of 16 hours of laboratory distributed in 8 sessions of two hours, that will realize in teams of two students, in the groups and schedules established to the effect by Ordinance of Studies and the Department of Electronic Engineering (EEL). The number of students in the internship sessions is limited to 15. The internships will be conducted in the Electronics Laboratory II, located on the 9th floor. Each practice is associated with a set of tasks to be performed as preliminary preparation.
The course material will be available on the Digital Campus.

LEARNING OBJECTIVES OF THE SUBJECT

It is a specialty subject that has four fundamental objectives:
1) CMOS process. The objective is to learn how an integrated circuit is designed and manufactured in CMOS technology. The technology for manufacturing nanometric CMOS processes and the materials and techniques used are studied.
2) Design at the level of physical layout. The objective is to introduce the digital design techniques. The semicustom and fullcustom techniques will be studied.
3) Present the historical and modern techniques for information encryption/decryption and the application of integrated circuit technology in modern ciphering.
4) Explaining the weaknesses that may exist in the integrated electronic ciphering systems and some countermeasures used.

STUDY LOAD

Type	Hours	Percentage
Hours small group	13,5	12.00
Self study	72,0	64.00
Hours large group	27,0	24.00

Total learning time: 112.5 h

CONTENTS

MI.T1. Reduction of scale and its advantages.

Description:
Domains and design levels. A little history. The integrated circuit. Current status and trends in electronics. Growth challenges. Scaling and technological limits of integration. Channel shortening. Scaling domains. Microelectronic Design Technologies. Beyond Moore.

Full-or-part-time: 2h 24m
Theory classes: 2h 24m

MI.T2. CMOS technologies.

Description:
Manufacturing alternatives on silicon. The MOS transistor. MOS transistor layout. Capabilities of the MOS structure. Technologies with MOS transistors. CMOS technologies. CMOS inverter. Static characteristics. Dynamic behavior. Delay. Consumption.

Full-or-part-time: 2h 24m
Theory classes: 2h 24m

MI.T3. CMOS manufacturing process.

Description:
Integrated circuit factories. White room. Si crystal formation (Czochralski method). Silicon wafers. Basic operations of the wafer process. Photolithography. Engraving. Oxidation. Dissemination. Ionic implantation. Deposition. Example of process masks of a CMOS inverter. Dice encapsulation.

Full-or-part-time: 2h 24m
Theory classes: 2h 24m

MI.T4. Fullcustom digital design techniques.

Description:
Layout-level design in CMOS technologies. Design tools. Design rules. Electrical characterization and estimation of benefits. Architecture and layout of logical doors. Design of complex combinational functions. Euler's path method.

Full-or-part-time: 2h 24m
Theory classes: 2h 24m

MI.T5. Beyond CMOS.

Description:
Manometric technologies and characteristics of short channel transistors. SOI technologies. Non-planar MOS technologies. FinFet transistors. Non-semiconductor devices. Carbonanotubs. Transistors with CNFETS nanotubes.

Full-or-part-time: 2h 24m
Theory classes: 2h 24m

MII.T1. Introduction to cryptography.

Description:
Security of people vs. information security (SdI). Importance of SdI in IoT technologies. Economic impact of SdI. Areas of interest. Encryption techniques for privacy, confidentiality and reliability.

Full-or-part-time: 3h
Theory classes: 3h

MII.T2. History of cryptography.

Description:
Historical perspective. Classic encryption. Engravings, Hieroglyphics, Steganography, Scythia, Caesar method and Polybius Square. Cryptographic analysis techniques. Methods of Al-Durayhim and Al-Qalqashandi. Poly-alphabetic methods. Alberti's record and Vigenére's cipher. Methods of electromechanical coding of information and encryption. Encryption between wars. Vernam system. Drums by Alexander Koch. Enigma machine.

Full-or-part-time: 3h
Theory classes: 3h

MII.T3. Fundamentals of cryptography, part I.

Description:
Modern cryptography. Concepts of sender, receiver and channel. Open and closed channel (safe). Encryption based on secret key. Key properties. Symmetrical and asymmetrical ciphers. Principle of Kerckhoffs. NIST Standards Agency. Classification of the best known encryption algorithms. Flow and block ciphers. DES, first standardized symmetric key algorithm. Encryption modes. OTP ciphers. Random numbers: properties and generators.

Full-or-part-time: 3h
Theory classes: 3h

MII.T4. Fundamentals of cryptography, part II.

Description:
Asymmetric encryption. Best known algorithms for asymmetric encryption. RSA algorithm. Public key distribution. Hash functions. Message authentication. Digital signature. Public key cryptography infrastructure.

Full-or-part-time: 3h
Theory classes: 3h

GRADING SYSTEM

The theoretical part will be evaluated through a continuous assessment grade obtained from the exercises proposed in class, a presentation on the project developed in module I of the subject and a final exam.
The practical part will be evaluated based on the practical classes taken in module II.
The grade in the acts will be the result of applying the following equation, rounded to the nearest decimal:
NFINAL = 0.20 NPP + 0.4 NPF + 0.2 NAP + 0.20 NAC
NPP: Presentation note, module I.
NPF: Final exam grade.
NAP: Note of practicals module II.
NAC: Continuous evaluation note, of theory deliverables.
The subject's reassessment process in July will be based on the theoretical content with a test with the same characteristics as the final exam. The new note will replace the NPF obtained in June.
Only those students who have grades of not present in the final exam of the course will be listed as not present at the events. No test grade will be saved for subsequent courses. No proof of previous courses is accepted.

EXAMINATION RULES.

The final exam of the subject will last 3 hours and will consist of a multiple-choice test. This test will cover the entire subject.
The student, to access the exam room, must present an official identification document.
Once the notes have been published, a claim period will be opened.

BIBLIOGRAPHY

Basic:
- Baker, R. Jacob. CMOS circuit design, layout, and simulation [on line]. 4th ed. Hoboken, New Jersey: IEEE Press, [2019] [Consultation: 15/01/2025]. Available on: https://onlinelibrary-wiley-com.recursos.biblioteca.upc.edu/doi/book/10.1002/9780470891179. ISBN 9781119481515.
- Rabaey, Jan M ; Chandrakasan, Anantha ; Nikolic, Borivoje. Circuitos integrados digitales : una perspectiva de diseño. 2a ed. Madrid [etc.]: Prentice Hall, cop. 2004. ISBN 8420541036.
- Weste, Neil H.E ; Daid Money Harris. CMOS VLSI design : a circuits and systems perspective. 4th ed. Boston: Addison Wesley, cop. 2011. ISBN 9780321547743.
- Fúster Sabater, Amparo. Técnicas criptográficas de protección de datos. 3ª ed. rev. y act. Madrid: Ra-ma, DL 2003. ISBN 8478975942.
- Verbauwhede, Ingrid M. R. Secure integrated circuits and systems [on line]. 1st ed. New York: Springer, 2010 [Consultation: 29/03/2023]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-0-387-71829-3. ISBN 9780387718279.

RESOURCES

Hyperlink:
- Simulador LTSPICE. https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html- Fitxers de tecnologia. http://cmosedu.com/cmos1/book.htm