Course guide
240IEE31 - 240IEE31 - Microcomputers

Last modified: 16/05/2023

Unit in charge: Barcelona School of Industrial Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: MASTER'S DEGREE IN INDUSTRIAL ENGINEERING (Syllabus 2014). (Optional subject).

Academic year: 2023 **ECTS Credits:** 4.5 **Languages:** English

LECTURER

Coordinating lecturer: Juan Antonio Carrasco López

Others: Juan Antonio Carrasco López

REQUIREMENTS

Basic concepts of computer architecture. Combinational design at the gate level including XOR and XNOR gates. Flip-flops, registers, counters, and shift registers. Binary, octal and hexadecimal representations of bit sequences. Natural binary code. Addition in natural binary code. Binary coded decimal (BCD) code. Familiarity with a high-level programming language including usage of libraries.

TEACHING METHODOLOGY

There will be theory/problem classes and 6 laboratory sessions. The theory/problems classes will take place on lective mondays and wednesdays from 15:00 to 16:30 in classroom B.2 of building H. The 6 laboratory sessions will take place on lective mondays in Laboratory II of the 9th floor of the H building.

LEARNING OBJECTIVES OF THE SUBJECT

To become acquainted with the architecture of a modern microcontroller. To become acquainted with the design of basic combinational and sequential arithmetic modules. To learn to program subroutines in assembler language for a modern microcontroller. To learn to develop simple applications based on a modern microcontroller using a dialect of the C programming language.

STUDY LOAD

Type	Hours	Percentage
Hours large group	27,0	24.00
Self study	72,0	64.00
Hours small group	13,5	12.00

Total learning time: 112.5 h

CONTENTS

Basic architecture of the PIC18F4520 microcontroller

Description:
PIC18F4520 features. Package. Architecture. Program memory. Instruction storage and access. Data memory. Processor. Execution unit. Instruction execution cycle. Pipelining. The access bank.

Full-or-part-time: 1h
Theory classes: 1h

Two's complement code

Description:
Binary code. Codeword. Domain of a code. Overflow. One's complement of a codeword. Two's complement of a codeword. Definition of two's complement code. Domain of two's complement code. Representation in two's complement code of -x from the representation of x with correctness proof. Addition in two's complement code and overflow condition with correctness proofs. Subtraction in two's complement code and overflow condition with correctness proofs.

Full-or-part-time: 1h 30m
Theory classes: 1h 30m

Incomplete instruction set

Description:
Flags. Byte-oriented instructions. Bit-oriented instructions. Control instructions. Literal instructions.

Full-or-part-time: 1h 30m
Theory classes: 1h 30m

Input/output ports of the PIC18F4520 microcontroller

Description:
Pins and basic behavior. Port A. Port B. Port C. Port D. Port E.

Full-or-part-time: 1h
Theory classes: 1h

Interrupts in the PIC18F4520 microcontroller

Description:
Basic concepts. Interrupt system of the PIC18F4520 microcontroller.

Full-or-part-time: 1h
Theory classes: 1h

The timer/counter Timer0 of the PIC18F4520 microcontroller

Description:
General features of timer/counter Timer0. Special function register T0CON. Operation as 8 bit timer/counter. Operation as 16 bit timer/counter.

Full-or-part-time: 1h
Theory classes: 1h

I2C bus standard and its implementation with the PIC18F4520 as a master

Description:
I2C bus standard. Implementation of the standard with PIC18F4520 as a master.

Full-or-part-time: 1h
Theory classes: 1h

C tutorial

Description:
Program structure. Basic syntax. Data types. Variables. Constants. Storage classes. Operators. Expressions. Decision making. Loops. Functions. Arrays. Pointers. Structures. Unions. Bit fields. Typedef. Output. Preprocessor commands. Dynamic memory allocation.

Full-or-part-time: 7h 30m
Theory classes: 7h 30m

C18 dialect

Description:
main function and emulating a C program without inputs. Basic integer and floating-point data types. printf function. Binary integer constants. Integer promotions. Anonymous structures. More important pragmas: sections, interrupts and configuration bits. Contents of the header file ConfigBits.h. Contents of the header file p18f4520.h. Useful macros.

Full-or-part-time: 1h 30m
Theory classes: 1h 30m

Assembler language and subroutine programming examples

Description:
Basic syntax of assembler language. Fourteen examples of subroutine programming.

Full-or-part-time: 3h
Theory classes: 3h

Design of an ALU based on a carry propagate adder and analysis of its static delay

Description:
Specification of the ALU. Design of a 16 bit carry propagate adder. Design of a 16 bit two's complement carry propagate adder. Design of a 16 bit two's complement carry propagate subtractor. Design of a 16 bit two's complement carry propagate adder/subtractor. Design of the ALU. Definition of the static delay of a combinational circuit. Theoretical results with proofs on the static delay of a combinational circuit. Static delay analysis. Static delay of the ALU.

Full-or-part-time: 1h 30m
Theory classes: 1h 30m

Carry propagate adders and carry lookahead adders and analysis of their static delays

Description:
Static delay of 16 bit carry propagate adder. Design of 16 bit carry lookahead adder. Static delay of carry lookahead adder.

Full-or-part-time: 1h 30m
Theory classes: 1h 30m

Design of an enhanced ALU based on a carry lookahead adder and analysis of its static delay

Description:
Design on enhanced ALU. Static delay of enhanced ALU.

Full-or-part-time: 1h
Theory classes: 1h

Design of a sequential Booth multiplier

Description:
Design of a 4 bit sequential Booth multiplier with correctness proof.

Full-or-part-time: 0h 30m
Theory classes: 0h 30m

Combinational multipliers using carry save adders

Description:
Binary combinational multipliers. 6 bit binary combinational multiplier with addition of partial products using carry save adders. 6 bit two's complement combinational multiplier with addition of partial products using carry save adders with correctness proof. 6 bit universal combinational multiplier with addition of partial products using carry save adders with correctness proof. 6 bit universal combinational multiplier with addition of partial products using carry save adders.

Full-or-part-time: 1h 30m
Theory classes: 1h 30m

Standard IEEE 754 for floating-point arithmetic

Description:
Overview. Formats for representation of real numbers. Representation of normalized numbers. Representation of remaining types of values. Rang. Rounding. Rounding modes. Management of exceptions. Invalid operation. Division by zero. Overflow. Underflow. Inexact result.

Full-or-part-time: 1h
Theory classes: 1h

Development of applications based on the PIC18F4520 microcontroller using a development board and the C18 programming language

Description:
Development of four applications emulating a C program without inputs. Development of an application lightening cyclically a set of LEDs with constant frequency. Development of an application lightening cyclically a set of LEDs with variable frequency. Development of an application lightening cyclically a set of LEDs with variable frequency using interrupts and the sleep state of the microcontroller. Development of a stopwatch application.

Full-or-part-time: 9h
Theory classes: 9h

GRADING SYSTEM

The evaluation of the subject will be based on a written partial exam, a written final exam and a grade corresponding to the laboratory sessions with weights of, respectively, 25%, 50% and 25%. The grade calculated in this way will be rounded to 0.1 points, with ties up, and will never be smaller than 0. The partial exam will cover the contents taught in the theory/problems classes until the week before the exam except those corresponding to the topics in the sets of slides S9 to S12, will last one and a half hours and will be held in the place and schedule established by the School. The final exam will cover all the contents taught in the theory/problems classes except those corresponding to the topics in the sets of slides S9 to S12, will last three hours and will be held in the place and schedule established by the School. The grade corresponding to the laboratory sessions will be proportional to the number of exercises solved correctly. Will have an evaluation of NA (Not Attended) only the students who do not attend the partial exam, do not attend the final exam and do not attend any laboratory session. The reevaluation exam, which students who have failed the subject have the right to take, will cover the contents of all the topics of the theory/problems classes except those corresponding to the sets of slides topics S10 to S12.

EXAMINATION RULES.

Students will be allowed to use in the partial exam, the final exam and the reevaluation final a pocket calculator and, in the case of the final and reevaluation exams, a short document that will be made accessible through ATENEA with a detailed description of the set of instructions of the microcontroller that will be explained in the theory/problems classes to help them to program a simple subroutine in assembly language. For the resolution of the programming exercises of the laboratory sessions, the students will have access to all the documentation and files published at ATENEA well in advance and will be allowed to access Wikipedia. The detection of acts of plagiarism during the partial exam, the final exam, the reevaluation exam, or the laboratory sessions will be penalized with a 0 in the corresponding grade.

BIBLIOGRAPHY

Complementary:
- Patterson, David A.; Hennessy, John L.. Computer organization and design: the hardware/software interface. 5th ed. Burlington: Elsevier Morgan Kaufmann, 2014. ISBN 9780124077263.

RESOURCES

Other resources:
Slide sets and and files for the lab sessions that will be made available through ATENEA.