Course guide
240IEE33 - 240IEE33 - Digital Electronic Systems

Last modified: 16/05/2023

Unit in charge: Barcelona School of Industrial Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: MASTER'S DEGREE IN INDUSTRIAL ENGINEERING (Syllabus 2014). (Optional subject).

Academic year: 2023 **ECTS Credits:** 4.5 **Languages:** Spanish

LECTURER

Coordinating lecturer: Moreno Eguilaz, Juan Manuel

Others: Moreno Eguilaz, Juan Manuel

PRIOR SKILLS

Analysis of digital circuits and systems

REQUIREMENTS

Basic knowlegde of digital electronics

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
CEEELECT1. Design electronic systems (mixed analogical and digital systems and micro-mechanical systems on silicon, digital systems based on discrete components, logical programable devices and/or microprocessors, electronic instrumentation systems and power electronic systems) and manage development projects and/or commercialization of electronic systems or development projects and/or commercialization of systems in which the electronic subsystems have an important specific weight.
CEEELECT3. Empower for the management of a product (¿product manager¿), technical management or innovative management of electronic products or which include electronic subsystems with an important specific weight.
CEEELECT2. Analyse, diagnose and maintain the electronic systems and manage the maintenance equipment of electronic systems or of systems in which the electronic subsystems have an important specific weight.

TEACHING METHODOLOGY

This course has an assigned load of 4.5 ECTS credits, which is equivalent to 112.5 student's working hours. 44 of these hours correspond to face-to-face activities (28.5 hours of theory and problem lectures, 12 hours of laboratory experiments, of which 3.5 hours of assessments). The remaining 68.5 hours correspond to non-classroom activities (24 hours to complete the laboratory experiments and 44.5 hours to study the theory).

The course is structured in two parts: a theory part and a laboratory part. Each one of these parts involves face-to-face activities, non-attending activities, and assessment activities.

Face-to-face activities of the theory part include 28.5 hours of lectures, where the above indicated content will be followed. These lectures will consist in theory lectures and problems and examples resolution and/or discussion, going from one activity to another at the discretion of the professor. The 28.5 hours of lectures are equivalent to 19 sessions of 1.5 hours. If the academic calendar does not allow these 19 sessions, some of them will last until 2 hours to make the total amount of 28.5 hours scheduled. Non-attending activities of the theory part consist in the study of the matter.

The laboratory part consists of a set of laboratory experiments . Face-to-face activities of the laboratory part consist in 6 laboratory sessions of 2 hours, which will be held at the Laboratory of Electronics III, located on the 9th floor, door 45. In these sessions, the above indicated content will be followed. Non-attending activities of the laboratory part, which are estimated in 24 hours, include finishing the laboratory experiments. The practical part will be made individually.

LEARNING OBJECTIVES OF THE SUBJECT

Understand the different characteristics and benefits of programmable logic devices in order to use them properly in the implementation of digital systems.
Knowing how to apply the design methodology of digital systems using different CAD tools, especially those based on the VHDL hardware description language.
Enable students to optimize the implementation of logic functions using two-level gate structures with a cost function depending on the own structure.
Enable students to design complex synchronous automata, including the use of partitioning techniques and hierarchical techniques, as well as simple asynchronous automata.
Knowing the methods used for verification and test to ensure the quality of digital electronic products.

STUDY LOAD

Type	Hours	Percentage
Hours large group	27,0	24.00
Self study	72,0	64.00
Hours small group	13,5	12.00

Total learning time: 112.5 h

CONTENTS

T1: Digital systems, logic gates and digital technologies (1.5 h)

Description:
Digital systems. Binary systems. Binary signals. Strength of binary signals. Conflict resolution. Digital systems structure. Logic gates. Digital integrated circuits. Output models of logic gates. Tri-state outputs. Open drain and open collector outputs. Wired logic. Digital technologies. CMOS technology. Structure and operation of CMOS basic gates. Characteristic parameters of digital technologies: power supplies, voltage levels, noise margin, propagation delays, power consumption, current levels, and fan-out. Schmitt trigger gates.

Full-or-part-time: 3h
Practical classes: 1h 30m
Self study : 1h 30m

T2: Programmable logic devices as an alternative for the implementation of digital systems hardware (3 h)

Description:
Alternatives for the implementation of digital systems: hardware, software, and combination of hardware and software (co-design). Alternatives for the implementation of the digital systems hardware: off-the-shelf integrated circuits, full-custom integrated circuits, standard cells, gate arrays, and programmable logic devices. Cost analysis. Migrations. ASICs, ASSPs and SoCs. IP modules. Flexibility in logic and connections as the basis of programmable logic devices. Technologies and programmability of programmable logic devices. Precursors of actual programmable logic devices: ROMs, PLAs, PALs and sequential PALs. PLDs: macrocells. CPLDs. CPLD families: complexities. LCAs: configurable logic blocks. FPGAs: additional functional blocks (memory blocks, multipliers, DSP blocks, PLLs) and I/O standards selection. FPGA families. PSoCs: CPUs and digital and/or analog peripherals. PSoC families. The Cyclone III family from Altera.

Full-or-part-time: 6h
Practical classes: 3h
Self study : 3h

T3: Digital systems hardware design methodology (1,5 h)

Description:
Digital systems hardware design methodology: specification, conception, edition, compilation, functional verification, placement, routing, delay extraction, temporal verification, masks / programming map obtaining, manufacturing / programming, fault verification. Defects and faults in integrated circuits manufacturing. Production test. ATEs (automatic test equipment). Test vectors. Fault models. Test vector coverage: fault simulators. CAD tools: editors, compilers, functional simulators, fitters, delay extractors, temporal simulators, delay analyzers, programmers. Hardware description languages (HDL). Hardware description types: behavioral, structural, and mixed. Simulators at hardware description level (RTL simulators). Automatic synthesizers. Programming / configuration of programmable logic devices. The JTAG standard.

Full-or-part-time: 3h
Practical classes: 1h 30m
Self study : 1h 30m

T4: The VHDL hardware description language (9 h)

Description:
Introduction. Areas of use: modeling and synthesis. Advantages. VHDL simulators: processes, transactions, events, signal resolution, macrotime, and microtime. Basic elements: entities and architectures. Element identifiers. Data types and subtypes. Data objects types. Ports or input/output signals. Operators. Values. Entity declarative part. Architecture declarative part. Architecture body. Concurrent sentences. Signal assignments. Components: declaration and instances. Libraries. Repetitive and conditional generation of concurrent sentences. Processes. Sequential sentences. Variable assignments. If, case and loop sentences. Subprograms: functions and procedures. Subprogram calls. Packages. Difference between structural and behavioral descriptions. Difference between signals and variables. Differences between modeling and synthesis. Implementation of combinatorial blocks. Implementation of finite state machines. Application example.

Full-or-part-time: 12h
Practical classes: 6h
Self study : 6h

T5: Extension of combinational systems (6 h)

Description:
Logic function specification. Quine-McCluskey tabular method for logic function minimization using two gate levels. Cost function when using PLAs. Cost function when using basic CMOS gates. Examples. Propagation delays. Examples. Glitches: origin, effects, precautions and solutions. Examples. Area / delay compromise in combinational circuits. Examples. Test vector generation for combinational circuits.

Full-or-part-time: 9h
Practical classes: 4h 30m
Self study : 4h 30m

T6: Extension of sequential systems (7,5 h)

Description:
Synchronous and asynchronous sequential systems. Advantages and disadvantages of synchronous and asynchronous sequential systems. Flip-flop characteristic times. Metastability. Synchronous sequential systems: asynchronous signals synchronization, clock signal skew, maximum operation frequency, robust implementation, automata partitioning, hierarchical automata. Examples. Asynchronous sequential systems without clock signal: the Huffman model. Automata implementation using asynchronous sequential systems without clock signal. Examples. Multi-clocked asynchronous sequential systems: advantages and precautions. Examples. Sequential system test.

Full-or-part-time: 12h
Practical classes: 6h
Self study : 6h

Laboratory experiments

Description:
Experiment 1: Introduction to digital system hardware design based on programmable logic devices (3.5 h + 5.5 h)
Experiment 2: Introduction to digital system hardware design using VHDL (2 h + 3 h)
Experiment 3: Design of an automaton for the automatic opening and closing of a door using VHDL (2 h + 2 h)
Experiment 4: Design of an automaton for reading a matrix keyboard using VHDL (2 h + 2 h)
Experiment 5: Design of a control System with a secret key for the automatic opening and closing of a door using VHDL (2 h + 2 h)

Full-or-part-time: 26h
Laboratory classes: 11h 30m
Self study : 14h 30m

Assessment

Description:
Two partial exams.

Full-or-part-time: 3h 30m
Practical classes: 3h 30m

GRADING SYSTEM

The theory part will be assessed through two individual exams: a first partial exam at the beginning of the second half of the semester, and a second partial exam when ending the semester. The theory part will be globally re-assessed through an extraordinary unique exam, which will be held after the end of the ordinary exams period of the spring semester.

The laboratory part will be assessed through the development and documentation of the laboratory experiments. The laboratory part will not be re-assessed after the end of the ordinary exams period of the spring semester. The last laboratory grades obtained in the semester or semesters allowing the re-assessment of the theory part will be used to calculate the grade appearing in the extraordinary academic record of students attending re-assessment.

The ordinary final course grade will be equal to the first of the following grades, rounded to the nearest tenth of a point, while the extraordinary final course grade will be equal to the following fourth possible final grade, rounded to the nearest tenth of a point:

Nfinal1 = 0.25 Npp1 + 0.50 Npp2 + 0.25 Nplab
Nfinal2 = 0.75 Nextr + 0.25 Nplab

Npp1: Grade of first partial exam
Npp2: Grade of second partial exam
Nlab: Grade of laboratory experiments
Nextr: Grade of extraordinary exam
Nfinal1: Final grade (formula 1)
Nfinal2: Final grade (formula 2)

Not presented will appear only in the academic record of students which have not attended any of the above-mentioned exams. The final course grade for those students that have attended at least one exam, but not all exams, will be calculated considering as zeroes the grades of the unattended exams. No grades will be kept on record for future semesters. No exams can be validated from the academic record of previous semesters.

EXAMINATION RULES.

The first partial exam of the theory part, which will consider the first theory chapters, will last an hour and a half. It will take place in one of the scheduled theory sessions of the course during the week immediately following the partial exams week.

The second partial exam of the theory part, which will consider the rest of the chapters, will last for two hours. It will be held on the date and time set by Studies Planning for the final exam of the course.

Each one of the laboratory experiments should be shown and delivered to the professor, at most, two teaching weeks after the last laboratory session scheduled for this experiment.

The extraordinary exam of the theory part, which will consider all the chapters, will last three hours. It will be held on the date and time set by Studies Planning for the extraordinary exam of the course.

The theory partial exams will consist in a set of short questions and problems.

Students may not bring any documentation, calculator, mass storage device information (floppy, CD, DVD, memory stick, etc.), nor communication device (cell phone, etc.) in any of the exams. Students must bring their identity card, passport or other official identification. Students violating these rules will be forced to leave the exam.

The grades of the exams will be published in the Digital Campus indicating the associated claim period.

BIBLIOGRAPHY

Basic:
- Jasinski, Ricardo. Effective coding with VHDL : principles and best practice. Cambridge, Massachusetts: The MIT Press, [2016]. ISBN 9780262034227.
- Hayes, John P. Introduction to digital logic design. Reading, Mass.: Addison-Wesley, cop. 1993. ISBN 0201154617.
- Hwang, Enoch O. Digital logic and microprocessor design with interfacing. International edition. Australia: Cengage Learning, [2018]. ISBN 9781305859470.
- Wakerly, John F; Ching Chuen, Jong ; Chang, Chip-Hong. Digital design : principles and practices. 4th ed.. Upper Saddle River, New Jersey: Pearson, cop. 2007. ISBN 9780132016117.
- Navabi, Zainalabedin. Digital design and implementation with field programmable devices [on line]. New York [etc.]: Springer, cop. 2005 [Consultation: 21/04/2023]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/b117975. ISBN 1402080115.

RESOURCES

Other resources:
Atenea