Course guide
270503 - ACAP - High Performance Computer Architecture

Last modified: 12/07/2024

Unit in charge: Barcelona School of Informatics
Teaching unit: 701 - DAC - Department of Computer Architecture.

Degree: MASTER'S DEGREE IN INFORMATICS ENGINEERING (Syllabus 2012). (Compulsory subject).

Academic year: 2024 **ECTS Credits:** 6.0 **Languages:** Spanish

LECTURER

Coordinating lecturer: JOSE M. LLABERIA GRIÑÓ

Others: Primer quadrimestre:
JOSE M. LLABERIA GRIÑÓ - 11, 12

PRIOR SKILLS

Combinational and sequential logic circuits. Operation of a computer: components, interconnections, exceptions and interrupts. Machine language: programming and data representation. Memory hierarchy: performance and mechanisms that support it. Operating Systems: address translation, interrupt and exception management

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
CTE1. Capability to model, design, define the architecture, implement, manage, operate, administrate and maintain applications, networks, systems, services and computer contents.
CTE6. Capability to design and evaluate operating systems and servers, and applications and systems based on distributed computing.
CTE7. Capability to understand and to apply advanced knowledge of high performance computing and numerical or computational methods to engineering problems.

Generical:
CG1. Capability to plan, calculate and design products, processes and facilities in all areas of Computer Science.
CG3. Capability to lead, plan and supervise multidisciplinary teams.
CG4. Capacity for mathematical modeling, calculation and simulation in technology and engineering companies centers, particularly in research, development and innovation tasks in all areas related to Informatics Engineering.
CG6. Capacity for general management, technical management and research projects management, development and innovation in companies and technology centers in the area of Computer Science.
CG8. Capability to apply the acquired knowledge and to solve problems in new or unfamiliar environments inside broad and multidisciplinary contexts, being able to integrate this knowledge.

Transversal:
CTR5. APPROPIATE ATTITUDE TOWARDS WORK: Capability to be motivated by professional achievement and to face new challenges, to have a broad vision of the possibilities of a career in the field of informatics engineering. Capability to be motivated by quality and continuous improvement, and to act strictly on professional development. Capability to adapt to technological or organizational changes. Capacity for working in absence of information and/or with time and/or resources constraints.

Basic:
CB6. Ability to apply the acquired knowledge and capacity for solving problems in new or unknown environments within broader (or multidisciplinary) contexts related to their area of study.

TEACHING METHODOLOGY

Classes of theory in which concepts are developed and there is student participation.
Classes of problems where they apply the concepts developed in the lectures and the active agent is the student.
Laboratory classes where they apply the concepts developed in class theory in a concrete example of the processor. The active agent is the learner and collaboration between the elements of the group is a means to increase or establish knowledge.
The course develops contructiva. That is, some of the concepts learned in grade and in each issue of course increases the knowledge and ability to understand, analyze and reason about aspects of a processor. This training is also quantitative.

LEARNING OBJECTIVES OF THE SUBJECT

1.Learn to apply pipelining and parallelism techniques in the processor design.
2.Training to evaluate the performance of a computing system when running applications.
3.Training to exploit the capabilities of a computer system and stand or hide weaknesses.
4.Training to design and evaluate the architecture to support efficiently the implementation of operating systems.
5.Training for using a hardware description language and its application in the specification of processor elements.

STUDY LOAD

Type	Hours	Percentage
Self study	96,0	64.00
Hours small group	14,0	9.33
Hours medium group	20,0	13.33
Hours large group	20,0	13.33

Total learning time: 150 h

CONTENTS

Computer and performance metrics

Description:
Constituent elements of a computer, functioning, memory hierarchy, multithreaded, energy and performance metrics

Pipelining and parallelism

Description:
Using pipelining and parallelism techniques to increase productivity. Resources

Pipelining instruction execution

Description:
Data path of a linear pipelined processor and control. Concept of data hazard and control hazard. Adequacy of semantics

Performance enhancement

Description:
Software and hardware techniques to reduce the number of stall cycles in a pipelined processor

Parallel pipelines and superscalar processors

Description:
Interpretation of instructions for execution latency greater than the initiation latency. Using the technique of parallelism to interpret instructions

Exceptions and interrupts

Description:
Requirements in the data path and control for supporting interrupts and exceptions

Multiprocessors

Description:
Elements of a multiprocessor system. Private caches. Interconnection network. Concepts of memory consistency and cache coherence.

VHDL hardware description language

Description:
Learning a hardware description language

ACTIVITIES

Hardware description language

Description:
Learning VHDL language to describe and simulate logic circuits. Description of basic components in the path of a data processor and its subsequent verification

Specific objectives:
5

Related competencies :
CTE1. Capability to model, design, define the architecture, implement, manage, operate, administrate and maintain applications, networks, systems, services and computer contents.
CTE7. Capability to understand and to apply advanced knowledge of high performance computing and numerical or computational methods to engineering problems.
CG8. Capability to apply the acquired knowledge and to solve problems in new or unfamiliar environments inside broad and multidisciplinary contexts, being able to integrate this knowledge.
CG1. Capability to plan, calculate and design products, processes and facilities in all areas of Computer Science.
CG3. Capability to lead, plan and supervise multidisciplinary teams.
CG6. Capacity for general management, technical management and research projects management, development and innovation in companies and technology centers in the area of Computer Science.

Full-or-part-time: 20h 30m
Laboratory classes: 4h 30m
Self study: 16h

Analysis of a series processor

Description:
Study the data path of a serial processor. Identify the parts of the data path used for each type of instruction. Analysis and calculation of delay for each type of instruction and determining the cycle time of processor

Specific objectives:
2

Related competencies :
CTE6. Capability to design and evaluate operating systems and servers, and applications and systems based on distributed computing.
CTE7. Capability to understand and to apply advanced knowledge of high performance computing and numerical or computational methods to engineering problems.
CG4. Capacity for mathematical modeling, calculation and simulation in technology and engineering companies centers, particularly in research, development and innovation tasks in all areas related to Informatics Engineering.
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Full-or-part-time: 9h
Laboratory classes: 3h
Self study: 6h

Designing control logic for a pipelined processor. Determining the cycle time

Description:
Analysis of the data path. Designing control logic for an operation that matches the semantics of machine language. Determining the cycle time

Specific objectives:
1

Related competencies :
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Full-or-part-time: 11h
Laboratory classes: 3h
Self study: 8h

Design of an enhanced processor

Description:
Design of a pipelined processor with bypasses to reduce stall cycles and the control logic

Specific objectives:
1, 3

Related competencies :
CTE1. Capability to model, design, define the architecture, implement, manage, operate, administrate and maintain applications, networks, systems, services and computer contents.
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Full-or-part-time: 10h
Laboratory classes: 3h
Self study: 7h

Computer and performance metrics

Description:
Development of item 1 of the course

Specific objectives:
2, 3

Related competencies :
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Full-or-part-time: 14h
Theory classes: 2h
Practical classes: 3h
Self study: 9h

Pipelining and parallelism

Description:
Development of item 2 of the course

Specific objectives:
1, 2

Related competencies :
CTE1. Capability to model, design, define the architecture, implement, manage, operate, administrate and maintain applications, networks, systems, services and computer contents.
CTE6. Capability to design and evaluate operating systems and servers, and applications and systems based on distributed computing.
CTE7. Capability to understand and to apply advanced knowledge of high performance computing and numerical or computational methods to engineering problems.
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Full-or-part-time: 12h 42m
Theory classes: 3h
Practical classes: 2h
Self study: 7h 42m

Pipelined instruction executions

Description:
Development of item 3 of the course

Specific objectives:
1, 2, 3

Related competencies :
CTE1. Capability to model, design, define the architecture, implement, manage, operate, administrate and maintain applications, networks, systems, services and computer contents.
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Full-or-part-time: 16h
Theory classes: 3h
Practical classes: 3h
Self study: 10h

Increased performance

Description:
Development of item 4 of the course

Specific objectives:
2, 3

Related competencies :
CTE6. Capability to design and evaluate operating systems and servers, and applications and systems based on distributed computing.
CTE7. Capability to understand and to apply advanced knowledge of high performance computing and numerical or computational methods to engineering problems.
CG4. Capacity for mathematical modeling, calculation and simulation in technology and engineering companies centers, particularly in research, development and innovation tasks in all areas related to Informatics Engineering.
CTR5. APPROPIATE ATTITUDE TOWARDS WORK: Capability to be motivated by professional achievement and to face new challenges, to have a broad vision of the possibilities of a career in the field of informatics engineering. Capability to be motivated by quality and continuous improvement, and to act strictly on professional development. Capability to adapt to technological or organizational changes. Capacity for working in absence of information and/or with time and/or resources constraints.

Full-or-part-time: 18h 30m
Self study: 11h 12m
Theory classes: 3h
Practical classes: 4h 18m

Parallel pipelines and superscalar processors

Description:
Development of item 5 of the course

Specific objectives:
1, 2, 3

Related competencies :
CTE1. Capability to model, design, define the architecture, implement, manage, operate, administrate and maintain applications, networks, systems, services and computer contents.
CTE6. Capability to design and evaluate operating systems and servers, and applications and systems based on distributed computing.
CTE7. Capability to understand and to apply advanced knowledge of high performance computing and numerical or computational methods to engineering problems.
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Full-or-part-time: 17h
Theory classes: 3h
Practical classes: 4h
Self study: 10h

Exceptions and interrupts

Description:
Development of item 6 of the course

Specific objectives:
2, 4

Related competencies :
CTE6. Capability to design and evaluate operating systems and servers, and applications and systems based on distributed computing.
CTE7. Capability to understand and to apply advanced knowledge of high performance computing and numerical or computational methods to engineering problems.
CG4. Capacity for mathematical modeling, calculation and simulation in technology and engineering companies centers, particularly in research, development and innovation tasks in all areas related to Informatics Engineering.
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Full-or-part-time: 9h
Theory classes: 1h
Practical classes: 1h
Self study: 7h

Multiprocessors

Description:
Development of item 7 of the subject

Specific objectives:
1, 2, 3

Related competencies :
CTE1. Capability to model, design, define the architecture, implement, manage, operate, administrate and maintain applications, networks, systems, services and computer contents.
CTE6. Capability to design and evaluate operating systems and servers, and applications and systems based on distributed computing.
CTE7. Capability to understand and to apply advanced knowledge of high performance computing and numerical or computational methods to engineering problems.
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Full-or-part-time: 7h 18m
Theory classes: 1h 18m
Practical classes: 2h
Self study: 4h

Final exam

Description:
Evaluation of the consolidation of the concepts presented during the course by responding to questions and problems of reasoning about concepts presented

Specific objectives:
1, 2, 3, 4

Related competencies :
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Full-or-part-time: 3h
Guided activities: 3h

Midterm exam

Description:
Assessment goal for the first three issues

Specific objectives:
1, 2, 3

Related competencies :
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Full-or-part-time: 1h
Guided activities: 1h

Midterm exam

Description:
Assessment goal for the first three issues

Specific objectives:
1, 2, 3

Related competencies :
CTE1. Capability to model, design, define the architecture, implement, manage, operate, administrate and maintain applications, networks, systems, services and computer contents.
CTE6. Capability to design and evaluate operating systems and servers, and applications and systems based on distributed computing.
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Full-or-part-time: 1h
Guided activities: 1h

GRADING SYSTEM

The powers have a weight proportional to the time spent in activities and they are evaluated indirectly based on midterm exam, final exam and laboratory.
The two midterm exams are performed simultaneously and are a single exam.
Midterm exam (P): Written test which evaluates the objectives for the first three issues.
Final exam (F): Written test which evaluates all objectives of the course.
Laboratory (L) is evaluated from the reports submitted in each of the practice sessions and, where appropriate, a personal interview.

The final note (NF) is calculated using the following expression:
NF = max (0.8 x F, (0.65 x F + 0.15 x P)) + 0.2 x L

BIBLIOGRAPHY

Basic:
- Capilano Computing Systems, Ltd. LogicWorks 5: interactive circuit design software. Pearson, Prentice Hall, 2004. ISBN 9780131456587.
- Hennessy, J.L.; Patterson, D.A. Organización y diseño de computadores: la interfaz hardware/software. 2a ed. McGraw-Hill, 1995. ISBN 8448118294.
- Hennessy, J.L.; Patterson, D.A. Computer architecture: a quantitative approach. Sixth ed. Elsevier/Morgan Kaufmann, 2019. ISBN 9780128119051.