Course guide
270616 - AVLSI - Algorithms for VLSI

Last modified: 13/07/2022

Unit in charge: Barcelona School of Informatics
Teaching unit: 723 - CS - Department of Computer Science.

Degree: MASTER'S DEGREE IN INNOVATION AND RESEARCH IN INFORMATICS (Syllabus 2012). (Optional subject).

Academic year: 2022 **ECTS Credits:** 6.0 **Languages:** English

LECTURER

Coordinating lecturer: JORDI CORTADELLA FORTUNY

Others: Primer quadrimestre:
JORDI CORTADELLA FORTUNY - 10

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
CEE3.1. Capability to identify computational barriers and to analyze the complexity of computational problems in different areas of science and technology as well as to represent high complexity problems in mathematical structures which can be treated effectively with algorithmic schemes.
CEE3.2. Capability to use a wide and varied spectrum of algorithmic resources to solve high difficulty algorithmic problems.
CEE3.3. Capability to understand the computational requirements of problems from non-informatics disciplines and to make significant contributions in multidisciplinary teams that use computing.

Generical:
CG1. Capability to apply the scientific method to study and analyse of phenomena and systems in any area of Computer Science, and in the conception, design and implementation of innovative and original solutions.
CG3. Capacity for mathematical modeling, calculation and experimental designing in technology and companies engineering centers, particularly in research and innovation in all areas of Computer Science.

Transversal:
CTR6. REASONING: Capacity for critical, logical and mathematical reasoning. Capability to solve problems in their area of study. Capacity for abstraction: the capability to create and use models that reflect real situations. Capability to design and implement simple experiments, and analyze and interpret their results. Capacity for analysis, synthesis and evaluation.

Basic:
CB6. Ability to apply the acquired knowledge and capacity for solving problems in new or unknown environments within broader (or multidisciplinary) contexts related to their area of study.
CB8. Capability to communicate their conclusions, and the knowledge and rationale underpinning these, to both skilled and unskilled public in a clear and unambiguous way.
CB9. Possession of the learning skills that enable the students to continue studying in a way that will be mainly self-directed or autonomous.

TEACHING METHODOLOGY

The theoretical content of the course is taught in the theory lectures. During the practical classes, practical examples are solved and different types of problems are proposed. These problems will have to be solved during the time of autonomous learning. An algorithmic project will also be proposed during the course. Students will have to solve and implement it during their time of autonomous learning.

LEARNING OBJECTIVES OF THE SUBJECT

STUDY LOAD

Type	Hours	Percentage
Hours large group	54,0	36.00
Self study	96,0	64.00

Total learning time: 150 h

CONTENTS

Introduction.

Description:
Integrated circuit fabrication. Layout layers and design rules. VLSI design flow. VLSI design styles.

Two-level logic synthesis

Description:
Boolean Algebras. Representation of Boolean functions. Quine-McCluskey algorithm. Heuristic logic minimization: Espresso.

Multi-level logic synthesis.

Description:
Kernel-based algebraic decomposition. AIG-based decomposition. Technology mapping for standard cells and FPGAs.

Formal verification

Description:
Binary Decision Diagrams. Combinational equivalence checking. Sequential equivalence checking. Model checking with temporal logic.

Partitioning and Floorplanning

Description:
Partitioning algorithms. Representation of floorplans. Slicing floorplans. Floorplanning algorithms.

Placement

Description:
Optimization objectives. Algorithms for global placement. Algorithms for legalization and detailed placement.

Global routing

Description:
Representation of routing regions. Algorithms for single-net and full-net routing.

Detailed routing

Description:
Horizontal and vertical constraint graphs. Channel routing. Switchbox routing. Over-the-cell routing.

ACTIVITIES

Learning the design flow of a VLSI circuit

Full-or-part-time: 4h
Theory classes: 2h
Self study: 2h

Learning of algorithms for logic synthesis

Full-or-part-time: 34h
Theory classes: 10h
Practical classes: 4h
Self study: 20h

Learning of techniques for formal verification of circuits

Full-or-part-time: 24h
Theory classes: 6h
Practical classes: 4h
Self study: 14h

Learning of techniques for circuit floorplanning and placement

Full-or-part-time: 32h
Theory classes: 8h
Practical classes: 4h
Self study: 20h

Learning of routing algorithms

Full-or-part-time: 32h
Theory classes: 10h
Practical classes: 6h
Self study: 16h

GRADING SYSTEM

Grade = 35% FP + 35% FT + 30% EX

FP = Final Project (graded from 0 to 10) in which each participant is required to develop a project on some algorithmic problem related to Electronic Design Automation, either proposed by the professor or by the student. The results of the project will have to be presented in class. The source code of the software will have to be delivered in some form such that the results of the project can be easily generated by executing the application.

FT = Final Test graded from (0 to 10) covering the contents of the course.

EX = Exercises assigned to the student and solved during the Autonomous Learning time. Two assignments will be delivered during the course (15% of the grade each one).

BIBLIOGRAPHY

Basic:
- Hachtel, G.D.; Somenzi, F. Logic synthesis and verification algorithms. Kluwer Academic Publishers, 1996. ISBN 0792397460.
- Alpert, C.J.; Metha, D.P.; Sapatnekar, S.S. (eds.). Handbook of algorithms for physical design automation. CRC : Taylor & Francis, 2009. ISBN 9780849372421.
- Wang, L.-T.; Chang, Y.-W.; Cheng, K.-T. (eds.). Electronic design automation: synthesis, verification, and test. Morgan Kaufmann Publishers/Elsevier, 2009. ISBN 9780123743640.