Course guide
270642 - PA - Processor Architecture

Last modified: 13/07/2022

Unit in charge: Barcelona School of Informatics
Teaching unit: 701 - DAC - Department of Computer Architecture.

Degree: MASTER'S DEGREE IN INNOVATION AND RESEARCH IN INFORMATICS (Syllabus 2012). (Optional subject).

Academic year: 2022 **ECTS Credits:** 6.0 **Languages:** English

LECTURER

Coordinating lecturer: ROGER ESPASA SANS

Others: Primer quadrimestre:
ROGER ESPASA SANS - 10

PRIOR SKILLS

Understanding of Digital System Design

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
CEE4.1. Capability to analyze, evaluate and design computers and to propose new techniques for improvement in its architecture.

Generical:
CG5. Capability to apply innovative solutions and make progress in the knowledge to exploit the new paradigms of computing, particularly in distributed environments.

Transversal:
CTR6. REASONING: Capacity for critical, logical and mathematical reasoning. Capability to solve problems in their area of study. Capacity for abstraction: the capability to create and use models that reflect real situations. Capability to design and implement simple experiments, and analyze and interpret their results. Capacity for analysis, synthesis and evaluation.

Basic:
CB6. Ability to apply the acquired knowledge and capacity for solving problems in new or unknown environments within broader (or multidisciplinary) contexts related to their area of study.

TEACHING METHODOLOGY

The main concepts of processor architecture will be introduced in the lectures. In the interactive problem-solving classes the students will participate into applying the concepts learned into real world designs. Finally, the students will complete their learning experience with the lab sessions where they will put in practice the concepts learned in the lectures and applied in the problem-solving classes.

LEARNING OBJECTIVES OF THE SUBJECT

1.Basic understanding of the processor microarchitecture.
2.Assessment the performance of a processor.
3.Understanding of concurrency techniques transparent to the programmer used by processors to reduce the execution time.
4.Knowledge of a hardware description language and application in the design of digital systems.

STUDY LOAD

Type	Hours	Percentage
Hours large group	18,0	12.00
Hours small group	18,0	12.00
Self study	96,0	64.00
Hours medium group	18,0	12.00

Total learning time: 150 h

CONTENTS

1. Von-Neumann Architecture and performance

Description:
Von Neumann machine, performance metrics and technology outlook

2. Linearly pipelined processor

Description:
Datapath. Structural, Control and Data Hazards.

3. Techniques to increase the number of instructions executed per unit of time

Description:
Static code planification, shortcircuits.

4. Techniques to reduce the effective latency of memory

Description:
Caches. Store and Load management.

5. Multicicle Pipelined Processor and Software Optimizations

Description:
Multicicle pipeline. Datapath with multiple pipelines. Software transformations to increase the instruction level parallelism.

Branch Prediction and Exception Handling

Description:
Static and Dynamic Branch Prediction. Speculative Execution, Precise Exception handling.

Superscalar and out-of-order processors

Description:
Register Renaming. Out-of-Order handling.

ACTIVITIES

Design Tools and Simulators

Description:
Learn the design and simulation tools. The student will cover the building blocks of the datapath of a microprocessor.

Specific objectives:
1, 2, 3, 4

Related competencies :
CG5. Capability to apply innovative solutions and make progress in the knowledge to exploit the new paradigms of computing, particularly in distributed environments.
CEE4.1. Capability to analyze, evaluate and design computers and to propose new techniques for improvement in its architecture.
CTR6. REASONING: Capacity for critical, logical and mathematical reasoning. Capability to solve problems in their area of study. Capacity for abstraction: the capability to create and use models that reflect real situations. Capability to design and implement simple experiments, and analyze and interpret their results. Capacity for analysis, synthesis and evaluation.
CB6. Ability to apply the acquired knowledge and capacity for solving problems in new or unknown environments within broader (or multidisciplinary) contexts related to their area of study.

Full-or-part-time: 24h
Laboratory classes: 8h
Self study: 16h

Basic architecture and performance metrics of the datapath of a microprocessor

Description:
Study the concepts associated to this chapter and solve the problems sets.

Specific objectives:
1, 2

Related competencies :
CEE4.1. Capability to analyze, evaluate and design computers and to propose new techniques for improvement in its architecture.
CTR6. REASONING: Capacity for critical, logical and mathematical reasoning. Capability to solve problems in their area of study. Capacity for abstraction: the capability to create and use models that reflect real situations. Capability to design and implement simple experiments, and analyze and interpret their results. Capacity for analysis, synthesis and evaluation.

Full-or-part-time: 30h
Theory classes: 4h
Practical classes: 2h
Laboratory classes: 4h
Self study: 20h

Techniques to speed-up the execution of the instructions

Description:
Learn the concepts explained in the theory sessions and solve the problem sets.

Specific objectives:
2, 3

Related competencies :
CG5. Capability to apply innovative solutions and make progress in the knowledge to exploit the new paradigms of computing, particularly in distributed environments.
CEE4.1. Capability to analyze, evaluate and design computers and to propose new techniques for improvement in its architecture.
CTR6. REASONING: Capacity for critical, logical and mathematical reasoning. Capability to solve problems in their area of study. Capacity for abstraction: the capability to create and use models that reflect real situations. Capability to design and implement simple experiments, and analyze and interpret their results. Capacity for analysis, synthesis and evaluation.

Full-or-part-time: 38h
Theory classes: 6h
Practical classes: 6h
Laboratory classes: 6h
Self study: 20h

Multicycle, Superscalar and Out-of-Order Processors.

Description:
Learn the concepts explained in the theory sessions and solve the problem sets.

Specific objectives:
2, 3

Related competencies :
CG5. Capability to apply innovative solutions and make progress in the knowledge to exploit the new paradigms of computing, particularly in distributed environments.
CEE4.1. Capability to analyze, evaluate and design computers and to propose new techniques for improvement in its architecture.
CTR6. REASONING: Capacity for critical, logical and mathematical reasoning. Capability to solve problems in their area of study. Capacity for abstraction: the capability to create and use models that reflect real situations. Capability to design and implement simple experiments, and analyze and interpret their results. Capacity for analysis, synthesis and evaluation.

Full-or-part-time: 36h
Theory classes: 8h
Practical classes: 8h
Self study: 20h

Exams/Tests (apart from the lab sessions)

Description:
Course exams and tests

Specific objectives:
1, 2, 3, 4

Related competencies :
CG5. Capability to apply innovative solutions and make progress in the knowledge to exploit the new paradigms of computing, particularly in distributed environments.
CEE4.1. Capability to analyze, evaluate and design computers and to propose new techniques for improvement in its architecture.
CTR6. REASONING: Capacity for critical, logical and mathematical reasoning. Capability to solve problems in their area of study. Capacity for abstraction: the capability to create and use models that reflect real situations. Capability to design and implement simple experiments, and analyze and interpret their results. Capacity for analysis, synthesis and evaluation.
CB6. Ability to apply the acquired knowledge and capacity for solving problems in new or unknown environments within broader (or multidisciplinary) contexts related to their area of study.

Full-or-part-time: 22h
Guided activities: 2h
Self study: 20h

GRADING SYSTEM

The course has two marks:
1) The final exam (F)
2) The microprocessor project (P) to be done in the Lab

The final mark will be computed as: 0,6 x P + 0,4 F.
The project requires at least a score of 5 points (out of 10), or the course will be failed.

BIBLIOGRAPHY

Basic:
- Hennessy, J.L.; Patterson, D.A. Computer architecture: a quantitative approach. 6th ed. Elsevier/Morgan Kaufmann, 2019. ISBN 9780128119051.
- Patterson, D.A.; Hennessy, J.L. Computer organization and design: the hardware/software interface. 5th ed. Elsevier Morgan Kaufmann, 2014. ISBN 0123744938.
- Patterson, D.A.; Hennessy, J.L. Computer organization and design: the hardware/software interface. 5th ed. Elsevier Morgan Kaufmann, 2014. ISBN 9780124077263.
- Hennessy, J.L.; Patterson, D.A. Computer architecture: a quantitative approach. 6th ed. Elsevier/Morgan Kaufmann, 2019. ISBN 9780128119051.

Complementary:
- Johnson, M. Superscalar microprocessor design. Prentice Hall, 1991. ISBN 0138756341.