Course guide
2706450 - PV - Processor Verification

Last modified: 30/01/2026

Unit in charge: Barcelona School of Informatics
Teaching unit: 701 - DAC - Department of Computer Architecture.

Degree: MASTER'S DEGREE IN INNOVATION AND RESEARCH IN INFORMATICS (Syllabus 2012). (Optional subject).

Academic year: 2025 **ECTS Credits:** 6.0 **Languages:** English

LECTURER

Coordinating lecturer:

Others:

PRIOR SKILLS

Concepts of digital circuit design.
Hardware description languages (HDL).
Programming and scripting.
Principles of computer architecture.

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
CEE4.1. Capability to analyze, evaluate and design computers and to propose new techniques for improvement in its architecture.

Generical:
CG4. Capacity for general and technical management of research, development and innovation projects, in companies and technology centers in the field of Informatics Engineering.

Transversal:
CTR3. TEAMWORK: Capacity of being able to work as a team member, either as a regular member or performing directive activities, in order to help the development of projects in a pragmatic manner and with sense of responsibility; capability to take into account the available resources.
CTR5. APPROPIATE ATTITUDE TOWARDS WORK: Capability to be motivated by professional achievement and to face new challenges, to have a broad vision of the possibilities of a career in the field of informatics engineering. Capability to be motivated by quality and continuous improvement, and to act strictly on professional development. Capability to adapt to technological or organizational changes. Capacity for working in absence of information and/or with time and/or resources constraints.

Basic:
CB7. Ability to integrate knowledges and handle the complexity of making judgments based on information which, being incomplete or limited, includes considerations on social and ethical responsibilities linked to the application of their knowledge and judgments.
CB8. Capability to communicate their conclusions, and the knowledge and rationale underpinning these, to both skilled and unskilled public in a clear and unambiguous way.

TEACHING METHODOLOGY

The main concepts of processor pre-silicon verification will be introduced in the lectures. The students will complete their learning experience with the lab sessions where they will put into practice the concepts learned in the lectures.

LEARNING OBJECTIVES OF THE SUBJECT

1.To understand and implement a verification plan and a testbench, and execute it.
2.To be able to provide and defend the verification plan and its execution phases.
3.To use the EDA tools required to accomplish the project.

STUDY LOAD

Type	Hours	Percentage
Self study	96,0	64.00
Hours large group	27,0	18.00
Hours small group	27,0	18.00

Total learning time: 150 h

CONTENTS

Introduction to pre-silicon verification

Description:
Why verification is critical in modern design. Overview of the verification flow. The role of verification in microprocessor design.

Verification planning and testbenches

Description:
Verification plan and coverage goals. Testbench architecture. Monitors, checkers, and scoreboards.

SystemVerilog for verification (SVV)

Description:
SystemVerilog basics for testbench design. Interfaces and clocking blocks. Randomization and constraints. Classes, inheritance, polymorphism. Transactions (TLM).

Directed and randomized tests

Description:
Directed test methodologies. Randomized test generation. Test coverage analysis. Debugging strategies. Stimulus variation. Predictability vs. randomness. Constraints in test generation.

Assertions and functional coverage

Description:
Immediate vs. concurrent assertions. SVA (SystemVerilog Assertions) syntax and examples. Functional coverage vs. code coverage. Coverage-driven verification.

Introduction to UVM (Universal Verification Methodology)

Description:
UVM goals and structure. UVM components. Factory, configuration, and objection mechanisms.

UVM testbenches and sequencing

Description:
UVM test phases and flow. Sequences and sequence items. Building reusable tests. Debugging and simulation output.

Processor-specific verification challenges

Description:
Verifying CPU pipelines and control logic. Instruction-level and architectural verification. Handling interrupts, exceptions, and hazards. ISA compliance testing.

Formal verification techniques

Description:
Model checking and theorem proving overview. Equivalence checking. Bounded model checking. Use cases and limitations in microprocessor design.

Performance and power verification

Description:
Power-aware simulation concepts. Functional vs. low-power states. Performance modeling.

Debug strategies and coverage closure

Description:
Interpreting functional/code coverage reports. Optimizing tests for coverage. Debugging techniques and waveform analysis.

Trends and real-case studies

Description:
Latest trends in verification (RISC-V, ML-driven verification, formal tools). Review of real CPU verification case studies.

Introduction to post-silicon validation

Description:
How errors are detected and fixed in real hardware. Tools and methodologies.

ACTIVITIES

Introduction to pre-silicon verification

Specific objectives:
1

Related competencies :
CG4. Capacity for general and technical management of research, development and innovation projects, in companies and technology centers in the field of Informatics Engineering.
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Full-or-part-time: 10h 24m
Theory classes: 3h
Laboratory classes: 3h 24m
Self study: 4h

Verification fundamentals

Specific objectives:
1, 3

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Full-or-part-time: 52h 54m
Theory classes: 8h
Laboratory classes: 16h 54m
Self study: 28h

Advanced verification frameworks

Specific objectives:
1, 3

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Full-or-part-time: 33h 24m
Theory classes: 6h
Laboratory classes: 3h 24m
Self study: 24h

Verification techniques and debugging

Specific objectives:
1, 3

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Full-or-part-time: 33h 18m
Theory classes: 6h
Laboratory classes: 3h 18m
Self study: 24h

Industry trends and post-silicon validation

Specific objectives:
1

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Full-or-part-time: 8h
Theory classes: 4h
Self study: 4h

Verification project

Specific objectives:
1, 2, 3

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Full-or-part-time: 12h
Self study: 12h

GRADING SYSTEM

The course has two marks:
1) The lab sessions (L)
2) Presentation of a verification project (P)

The final mark will be computed as: 0,4 x L + 0,6 x P

BIBLIOGRAPHY

Basic:
- Spear, Chris ; Tumbush, Greg. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features. Springer Nature, 3rd ed. 2012. ISBN 9781461407157.
- Salemi, Ray. The UVM primer : an introduction to the Universal Verification Methodology. Boston Light Press, 2013. ISBN 9780974164939.