220117 - Digital Electronics

Coordinating unit: 205 - ESEIAAT - Terrassa School of Industrial, Aerospace and Audiovisual Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering
Academic year: 2019
Degree: BACHELOR'S DEGREE IN INDUSTRIAL TECHNOLOGY ENGINEERING (Syllabus 2010). (Teaching unit Compulsory)
ECTS credits: 6
Teaching languages: Catalan, Spanish

Teaching staff
Coordinator: Ortega Redondo, Juan Antonio
Others: Salaet Pereira, Juan Fernando
Capellá Frau, Gabriel José

Prior skills
It is recommended to have studied the Electronics course.

Degree competences to which the subject contributes

Specific:
1. An understanding of the fundamentals and applications of digital electronics and microprocessors

Transversal:
2. EFFECTIVE USE OF INFORMATION RESOURCES - Level 3. Planning and using the information necessary for an academic assignment (a final thesis, for example) based on a critical appraisal of the information resources used.

Teaching methodology
1. Large group: These classes develop theoretical concepts, some problems, and evaluations for the first and second set level tests. We will use the exhibition model that the teacher sees fit to assimilate the objectives that have been set in the subject.
2. Small groups: This activity will develop laboratory sessions.
ATHENA platform will be used as a support tool in the two types of classes

Learning objectives of the subject
1. Understanding and mastering the basics of the digital systems analysis and design.
2. Knowledge of hardware description languages and their application to the design of digital systems.
4. Knowledge and domain of embedded systems design (System on Chip) and its application in real systems.
## 220117 - Digital Electronics

### Study load

<table>
<thead>
<tr>
<th>Total learning time: 150h</th>
<th>Hours large group: 46h</th>
<th>30.67%</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Hours small group: 14h</td>
<td>9.33%</td>
</tr>
<tr>
<td></td>
<td>Self study: 90h</td>
<td>60.00%</td>
</tr>
</tbody>
</table>
# 220117 - Digital Electronics

## Content

<table>
<thead>
<tr>
<th>1.- Digital system description. From zero to one</th>
<th>Learning time: 14h</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Description:</strong></td>
<td>Theory classes: 6h</td>
</tr>
<tr>
<td>1.1.- An historic perspective.</td>
<td>Laboratory classes: 2h</td>
</tr>
<tr>
<td>1.2.- Description levels.</td>
<td>Self study: 6h</td>
</tr>
<tr>
<td>1.3.- The Art of Managing Complexity</td>
<td></td>
</tr>
<tr>
<td>1.3.- The Digital Abstraction</td>
<td></td>
</tr>
<tr>
<td>1.4.- Number Systems</td>
<td></td>
</tr>
<tr>
<td>1.5.- Logic Gates</td>
<td></td>
</tr>
<tr>
<td>1.6.- Logic Levels</td>
<td></td>
</tr>
<tr>
<td>1.7.- CMOS Transistors</td>
<td></td>
</tr>
<tr>
<td>1.8.- Power Consumption.</td>
<td></td>
</tr>
<tr>
<td><strong>Related activities:</strong></td>
<td></td>
</tr>
<tr>
<td>Theory classes, problems and laboratory.</td>
<td></td>
</tr>
<tr>
<td>Individual test: knowledge about Boolean algebra.</td>
<td></td>
</tr>
<tr>
<td>Laboratory: Digital system design. Complete process.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>2.- Combinational Logic Design</th>
<th>Learning time: 17h 30m</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Description:</strong></td>
<td>Theory classes: 3h 30m</td>
</tr>
<tr>
<td>2.1.- Introduction</td>
<td>Laboratory classes: 2h</td>
</tr>
<tr>
<td>2.2.- Boolean Equations</td>
<td>Self study: 12h</td>
</tr>
<tr>
<td>2.3.- Boolean Algebra</td>
<td></td>
</tr>
<tr>
<td>2.4.- From Logic to Gates</td>
<td></td>
</tr>
<tr>
<td>2.5.- Multilevel Combinational Logic</td>
<td></td>
</tr>
<tr>
<td>2.6.- X's and Z's</td>
<td></td>
</tr>
<tr>
<td>2.7.- Karnaugh Maps</td>
<td></td>
</tr>
<tr>
<td>2.8.- Combinational Building Blocks</td>
<td></td>
</tr>
<tr>
<td>2.9.- Timing</td>
<td></td>
</tr>
<tr>
<td><strong>Related activities:</strong></td>
<td></td>
</tr>
<tr>
<td>Theory classes, problems and laboratory.</td>
<td></td>
</tr>
<tr>
<td>Laboratory: Digital system design. The adder.</td>
<td></td>
</tr>
</tbody>
</table>
### 3. Sequential Logic Design

**Description:**
- 3.1.- Introduction
- 3.2.- Latches and Flip-Flops
- 3.3.- Synchronous Logic Design
- 3.4.- Finite State Machines
- 3.5.- Timing of Sequential Logic
- 3.6.- Parallelism

**Related activities:**
Theory classes, problems and laboratory. 
Laboratory: Sequential digital system design: Chronometer.

**Learning time:** 21h
- Theory classes: 4h
- Laboratory classes: 2h
- Self study: 15h

### 4. Hardware Description Languages

**Description:**
- 4.1.- Introduction
- 4.2.- Combinational Logic
- 4.3.- Structural Modeling
- 4.4.- Sequential Logic
- 4.5.- More Combinational Logic
- 4.6.- Finite State Machines
- 4.7.- Parameterized Modules
- 4.8.- Testbenches

**Related activities:**
Theory classes, problems and laboratory. 
Laboratory: Design of complex systems.

**Learning time:** 27h 30m
- Theory classes: 5h 30m
- Laboratory classes: 2h
- Self study: 20h

First exam, contents: 1, 2, 3 and 4.
5.- Architecture of microprocessors based systems

**Description:**
5.1 Introduction
5.2 Assembly Language
5.3 Machine Language
5.4 Programming
5.5 Addressing Modes
5.6 Lights, Camera, Action: Compiling, Assembling, and Loading
5.7 Odds and Ends
5.8 Real World Perspective: IA-32 Architecture

**Related activities:**
Theory classes, problems and laboratory.

---

**Learning time:** 43h
- Theory classes: 20h
- Laboratory classes: 4h
- Self study: 19h

6.- Input and output transfers. Peripherals

**Description:**
6.1 Introduction
6.2 Synchronization by pooling
6.3 Synchronization by interrupt
6.4 Timers and counters
6.5 Serial communication interfaces
6.6 A/D Converters

**Related activities:**
Theory classes, problems and laboratory.

---

**Learning time:** 27h
- Theory classes: 7h
- Laboratory classes: 2h
- Self study: 18h

---

**Qualification system**

- Partial exam N1P weight: 35%
- Final exam N2P weight: 35%
- Lab NL- weight: 30%

The unsatisfactory results of the partial exam may be recovered through a written test to be done on the day set for the final exam. This test can be accessed by students with a mark less than 5.0 of the partial exam. The recover test will be evaluated with a rating between 0 and 5. The mark obtained by applying the recovery will replace the initial qualification as long as it is superior.
220117 - Digital Electronics

Bibliography

Basic:


Complementary: