Course guide
230019 - DGD - Digital Design

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.
Degree: BACHELOR'S DEGREE IN TELECOMMUNICATIONS TECHNOLOGIES AND SERVICES ENGINEERING (Syllabus 2015). (Compulsory subject).
BACHELOR'S DEGREE IN DATA SCIENCE AND ENGINEERING (Syllabus 2017). (Optional subject).
Academic year: 2022
ECTS Credits: 6.0
Languages: Catalan

LECTURER
Coordinating lecturer: Consultar aquí / See here: https://telecos.upc.edu/ca/estudis/curs-actual/professorat-responsables-coordinadors/responsables-assignatura
Others: Consultar aquí / See here: https://telecos.upc.edu/ca/estudis/curs-actual/professorat-responsables-coordinadors/professorat-assignat-idioma

PRIOR SKILLS
Basic analysis of electronic circuits.
Basic knowledge of electronic devices and, in particular, the MOS transistor.

REQUIREMENTS
FONAMENTS D'ELECTRÒNICA - Precorequisit

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES
Generical:
12 CPE N2. They will be able to identify, formulate and solve engineering problems in the ICC field and will know how to develop a method for analysing and solving problems that is systematic, critical and creative.

TEACHING METHODOLOGY
Lectures and application classes
Laboratory classes
Group work (distance)
Individual work (distance)
Exercises
Short answer tests (Control)
Long answer tests (Final Exam)
Laboratory work

LEARNING OBJECTIVES OF THE SUBJECT
The student must be able to analyze, design and experimentally verify combinational and sequential digital subsystems. This course introduces and uses the hardware description language VHDL. It also includes an introduction to CMOS logic circuits, an introduction and utilización of programmable logic devices and an introduction to complex digital systems.
STUDY LOAD

<table>
<thead>
<tr>
<th>Type</th>
<th>Hours</th>
<th>Percentage</th>
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</thead>
<tbody>
<tr>
<td>Hours small group</td>
<td>26,0</td>
<td>17.33</td>
</tr>
<tr>
<td>Self study</td>
<td>85,0</td>
<td>56.67</td>
</tr>
<tr>
<td>Hours large group</td>
<td>39,0</td>
<td>26.00</td>
</tr>
</tbody>
</table>

Total learning time: 150 h

CONTENTS

**Module 1. Introduction to digital design**

**Description:**
The digital abstraction, systems and digital signals, behavior vs. structure, hierarchical design. Logic functions and Boolean algebra. Number systems and codes. Under the digital abstraction: power, delay, power consumption, logic levels and high impedance.

**Full-or-part-time:** 17h
Theory classes: 7h
Self study : 10h

**Module 2. Combinational design**

**Description:**
SdP and PdS canonic design. Simplification of logic functions. Combinational design based on logic gates and on standard combinational modules. Multiplexers, decoders, adders, comparators, etc.

**Full-or-part-time:** 30h
Theory classes: 10h
Laboratory classes: 2h
Self study : 18h

**Module 3. Combinational design with VHDL**

**Description:**
History and basic features of HDLs, methodologies and design tools. Basic elements: data types, objects, operators. Units Description: entities, architectures, packages and libraries. Concurrent assignments, conditional assignments and selections. Processes and sequential statements. Declaration and instantiation of components.

**Full-or-part-time:** 24h
Theory classes: 6h
Laboratory classes: 4h
Self study : 14h
Module 4. Sequential design

**Description:**

**Full-or-part-time:** 55h
- Theory classes: 15h
- Laboratory classes: 10h
- Self study: 30h

Module 5. CMOS digital circuits

**Description:**
Types of digital ICs and logic families. MOS transistors. CMOS inverter and basic logic gates. CMOS features: circuit delays, spurious, static and dynamic power consumption. Programmable logic devices, logic cells, and types of synthesis. Memory structures.

**Full-or-part-time:** 22h
- Theory classes: 10h
- Self study: 12h

**GRADING SYSTEM**

Final grade based on the respective qualifications of the theory (60%) and the laboratory (40%) parts. The theory mark consists of 60% from the final theory exam and 40% from continuous assessment: exams, small works, delivery of problems or other activities done during the course. The laboratory mark is obtained from the laboratory work done during the course and from the final lab exam.

The re-evaluation of the course involves having to do the final exam again, which includes theory and laboratory parts. Grades earned replace the previous ones. Laboratory work and continuous assessment are not re-avaluable.

**EXAMINATION RULES.**

During the exams it is not allowed to use wireless devices (mobile phones, laptops, tablets, etc..) nor programmable calculators. It is also necessary to provide some identification document (ID card, passport, etc.)

**BIBLIOGRAPHY**

**Basic:**

**RESOURCES**

**Computer material:**
- Quartus II Web edition