230019 - DGD - Digital Design

Coordinating unit: 230 - ETSETB - Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering
Academic year: 2019
Degree:
BACHELOR'S DEGREE IN TELECOMMUNICATIONS TECHNOLOGIES AND SERVICES ENGINEERING (Syllabus 2015). (Teaching unit Compulsory)
BACHELOR'S DEGREE IN AUDIOVISUAL SYSTEMS ENGINEERING (Syllabus 2009). (Teaching unit Compulsory)
BACHELOR'S DEGREE IN ELECTRONIC SYSTEMS ENGINEERING (Syllabus 2009). (Teaching unit Compulsory)
BACHELOR'S DEGREE IN TELECOMMUNICATIONS SCIENCE AND TECHNOLOGY (Syllabus 2010). (Teaching unit Compulsory)
BACHELOR'S DEGREE IN TELECOMMUNICATIONS SYSTEMS ENGINEERING (Syllabus 2010). (Teaching unit Compulsory)
BACHELOR'S DEGREE IN NETWORK ENGINEERING (Syllabus 2010). (Teaching unit Compulsory)
ECTS credits: 6
Teaching languages: Catalan

Teaching staff

Coordinator: Pons Nin, Joan
Mateo Peña, Diego
Others: Altet, Josep
Bardés, Daniel
Bermejo, Sandra
Calderer, Josep
Chávez, Juan Antonio
Garcies, Pau
Martín, Isidro
Mateo, Diego
Pons, Joan
Puigdollers, Joaquim

Prior skills

Basic analysis of electronic circuits.
Basic knowledge of electronic devices and, in particular, the MOS transistor.

Requirements

Electronics Fundamentals
Linear Circuits

Degree competences to which the subject contributes

Generical:
12 CPE N2. They will be able to identify, formulate and solve engineering problems in the ICC field and will know how to develop a method for analysing and solving problems that is systematic, critical and creative.
The student must be able to analyze, design and experimentally verify combinational and sequential digital subsystems. This course introduces and uses the hardware description language VHDL. It also includes an introduction to CMOS logic circuits, an introduction and utilization of programmable logic devices and an introduction to complex digital systems.

<table>
<thead>
<tr>
<th>Study load</th>
<th>Total learning time: 150h</th>
<th>Hours large group: 39h</th>
<th>26.00%</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Hours small group: 26h</td>
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<td>17.33%</td>
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<tr>
<td></td>
<td>Self study: 85h</td>
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<td>56.67%</td>
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# Content

## Module 1. Introduction to digital design

**Learning time:** 17h  
Theory classes: 7h  
Self study: 10h

**Description:**  
The digital abstraction, systems and digital signals, behavior vs. structure, hierarchical design. Logic functions and Boolean algebra. Number systems and codes. Under the digital abstraction: power, delay, power consumption, logic levels and high impedance.

## Module 2. Combinational design

**Learning time:** 30h  
Theory classes: 10h  
Laboratory classes: 2h  
Self study: 18h

**Description:**  
SDP and PD5 canonic design. Simplification of logic functions. Combinational design based on logic gates and on standard combinational modules. Multiplexers, decoders, adders, comparators, etc.

## Module 3. Combinational design with VHDL

**Learning time:** 24h  
Theory classes: 6h  
Laboratory classes: 4h  
Self study: 14h

**Description:**  
History and basic features of HDLs, methodologies and design tools. Basic elements: data types, objects, operators. Units Description: entities, architectures, packages and libraries. Concurrent assignments, conditional assignments and selections. Processes and sequential statements. Declaration and instantiation of components.

## Module 4. Sequential design

**Learning time:** 55h  
Theory classes: 15h  
Laboratory classes: 10h  
Self study: 30h

**Description:**  
Module 5. CMOS digital circuits

Learning time: 22h
- Theory classes: 10h
- Laboratory classes: 0h
- Self study: 12h

Description:
Types of digital ICs and logic families. MOS transistors. CMOS inverter and basic logic gates. CMOS features: circuit delays, spurious, static and dynamic power consumption. Programmable logic devices, logic cells, and types of synthesis. Memory structures.

Qualification system

Final grade based on the respective qualifications of the theory (60%) and the laboratory (40%) parts. The theory mark consists of 60% from the final theory exam and 40% from continuous assessment: exams, small works, delivery of problems or other activities done during the course. The laboratory mark is obtained from the laboratory work done during the course and from the final lab exam.

The re-evaluation of the course involves having to do the final exam again, which includes theory and laboratory parts. Grades earned replace the previous ones. Laboratory work and continuous assessment are not re-avaluable.

This course will assess the generic skill:
- Ability to identify, formulate and solve engineering problems (Intermediate Level)

Regulations for carrying out activities

During the exams it is not allowed to use wireless devices (mobile phones, laptops, tablets, etc..) nor programmable calculators. It is also necessary to provide some identification document (ID card, passport, etc.)

Bibliography

Basic:

Others resources:
- Computer material
- Quartus II Web edition