Last update: 06-05-2019

230091 - DSBM - Systems Based on Microprocessors Design

Coordinating unit: 230 - ETSETB - Barcelona School of Telecommunications Engineering

Teaching unit: 710 - EEL - Department of Electronic Engineering

Academic year: 2019

Degree: BACHELOR'S DEGREE IN TELECOMMUNICATIONS TECHNOLOGIES AND SERVICES ENGINEERING (Syllabus 2015). (Teaching unit Compulsory)

ECTS credits: 6 Teaching languages: Catalan

Teaching staff

Coordinator: Jimenez Serres, Vicente

Others: Dominguez Pumar, Manuel M.
Salazar Soler, Jorge
Bardes Llorensi, Daniel
Pol Fernandez, Clemente
Madrenas Boadas, Jordi

Degree competences to which the subject contributes

Transversal:

07 AAT N2. SELF-DIRECTED LEARNING - Level 2: Completing set tasks based on the guidelines set by lecturers. Devoting the time needed to complete each task, including personal contributions and expanding on the recommended information sources.

Teaching methodology

Lectures
Laboratory sessions
Team assignments (at home)
Individual work
Continuous assessment evaluation
Final assessment evaluation

Learning objectives of the subject

Programming, analysis and design of microprocessor / microcontroller based systems.

Study load

Total learning time: 150h	Hours large group:	39h	26.00%
	Hours small group:	26h	17.33%
	Self study:	85h	56.67%

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Content

T1-Introduction

Learning time: 1h 58m
Theory classes: 1h
Self study : 0h 58m

Description:
Subject description. Digital electronics context. Digital implementation options. Basic CPU system structure. Software execution.

T2-Compilation and debugging

Learning time: 5h 50m
Theory classes: 3h
Self study : 2h 50m

Description:
Software and Firmware. Code generation. Code load. Debugging.

T3-Electrical compatibility

Learning time: 14h 28m
Theory classes: 5h
Self study : 9h 28m

Description:
Static and dynamic characteristics. Requirements and performance parameters. Compatibility in interconnections. Buses. Usage of open collector/drain in busses.

T4-The CPU

Learning time: 13h 36m
Theory classes: 7h
Self study : 6h 36m

Description:
Control unit and datapath. Von Neumann and Harvard structures. Instruction cycle. Microprogram. Speed and power metrics. CPU optimization. External buses. Endianness.
Memory hierarchy. Cache memory. Protection and virtual memory.

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T5-Memory subsystem	Learning time: 14h 28m Theory classes: 5h Self study : 9h 28m

Description:
Memory classification. Typical SRAM and ROM signals. Decoding. DRAM memories and others.

T6-Timing	Learning time: 14h 28m Theory classes: 5h Self study : 9h 28m

Description:
content english

Specific objectives:
Requirements to evaluate. Timing and read/write evaluation. DRAM timing.

T7-Input/Output	Learning time: 11h 40m Theory classes: 6h Self study : 5h 40m

Description:
Peripheral connections. I/O map. Registers. Polling and interrupt synchronization. RSIs. Execution context. Masking. Latency. Exceptions. Peripheral examples: Timers, Converters, Communications.

T8-Programming model	Learning time: 4h 20m Theory classes: 1h 30m Self study : 2h 50m

Description:
Tasks and events. CPU usage. Operating systems. Processes. Real time systems. Scheduling. Process synchronization.

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Laboratory	Learning time: 58h Laboratory classes: 26h Self study : 32h

Description:
ARM Cortex M4 system development. Development environment. Peripheral access. Interrupts. Timing measurements. Threads.

Qualification system

50% Final exam
30% Laboratory sessions
20% Continuous assessment evaluation

Bibliography

Basic:

Clements, Alan. Microprocessor systems design : 68000 hardware, software, and interfacing. 3rd ed. Boston [etc.]: PWS, cop. 1997. ISBN 0534948227.

Cabestany, J.; Madrenas, J.; Masana F.; Salazar, J. ; Pol, C.. Disseny de sistemes digitals amb microprocessadors [on line]. 2a ed. Barcelona: Edicions UPC, 2000Available on: <http://hdl.handle.net/2099.3/36234>. ISBN 8483013657.

Complementary:

Li, Qing; Yao, Caroline. Real-Time concepts for embedded systems. San Francisco: CMPBooks, cop. 2003. ISBN 1578201241.

Tanenbaum, Andrew S. Structured computer organization. 5th ed. Upper Saddle River, Prentice Hall, cop. 2006. ISBN 978-0131485211.

Catsoulis, J. Designing embedded hardware [on line]. 2nd ed. Beijing [etc.]: O'Reilly, 2005 [Consultation: 19/02/2019]. Available on: <https://ebookcentral.proquest.com/lib/upcatalunya-ebooks/detail.action?docID=540710>. ISBN 9780596007553.