230091 - DSBM - Systems Based on Microprocessors Design

Coordinating unit: 230 - ETSETB - Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering
Academic year: 2018
Degree: BACHELOR'S DEGREE IN TELECOMMUNICATIONS TECHNOLOGIES AND SERVICES ENGINEERING (Syllabus 2015). (Teaching unit Compulsory)
ECTS credits: 6
Teaching languages: Catalan

Teaching staff

Coordinator: Jimenez Serres, Vicente
Others: Dominguez Pumar, Manuel M.
Salazar Soler, Jorge
Bardes Llorensi, Daniel
Pol Fernandez, Clemente
Madrenas Boadas, Jordi

Degree competences to which the subject contributes

Transversal:
07 AAT N2. SELF-DIRECTED LEARNING - Level 2: Completing set tasks based on the guidelines set by lecturers. Devoting the time needed to complete each task, including personal contributions and expanding on the recommended information sources.

Teaching methodology

Lectures
Laboratory sessions
Team assignments (at home)
Individual work
Continuous assessment evaluation
Final assessment evaluation

Learning objectives of the subject

Programming, analysis and design of microprocessor / microcontroller based systems.

Study load

<table>
<thead>
<tr>
<th>Total learning time: 150h</th>
<th>Hours large group: 39h</th>
<th>26.00%</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Hours small group: 26h</td>
<td>17.33%</td>
</tr>
<tr>
<td></td>
<td>Self study: 85h</td>
<td>56.67%</td>
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</tbody>
</table>
## 230091 - DSBM - Systems Based on Microprocessors Design

### Content

<table>
<thead>
<tr>
<th>Topic</th>
<th>Learning time:</th>
<th>Theory classes:</th>
<th>Self study:</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>T1-Introduction</strong></td>
<td>1h 58m</td>
<td>1h</td>
<td>0h 58m</td>
</tr>
<tr>
<td><strong>Description:</strong></td>
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<tr>
<td>Subject description. Digital electronics context. Digital implementation options. Basic CPU system structure. Software execution.</td>
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</table>

| **T2-Compilation and debugging**   | 5h 50m          | 3h              | 2h 50m      |
| **Description:**                   |                 |                 |             |

| **T3-Electrical compatibility**    | 14h 28m         | 5h              | 9h 28m      |
| **Description:**                   |                 |                 |             |

| **T4-The CPU**                     | 13h 36m         | 7h              | 6h 36m      |
| **Description:**                   |                 |                 |             |
### T5-Memory subsystem

**Description:**
Memory classification. Typical SRAM and ROM signals. Decoding. DRAM memories and others.

**Learning time:** 14h 28m
- Theory classes: 5h
- Self study: 9h 28m

### T6-Timing

**Description:**
- Content: English

**Specific objectives:**
Requirements to evaluate. Timing and read/write evaluation. DRAM timing.

**Learning time:** 14h 28m
- Theory classes: 5h
- Self study: 9h 28m

### T7-Input/Output

**Description:**

**Learning time:** 11h 40m
- Theory classes: 6h
- Self study: 5h 40m

### T8-Programming model

**Description:**

**Learning time:** 4h 20m
- Theory classes: 1h 30m
- Self study: 2h 50m
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<table>
<thead>
<tr>
<th>Laboratory</th>
<th>Learning time: 58h</th>
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<tbody>
<tr>
<td></td>
<td>Laboratory classes: 26h</td>
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<tr>
<td></td>
<td>Self study: 32h</td>
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</tbody>
</table>

**Description:**

**Qualification system**
50% Final exam
30% Laboratory sessions
20% Continuous assessment evaluation

**Bibliography**

**Basic:**


**Complementary:**