230091 - DSBM - Systems Based on Microprocessors Design

Coordinating unit: 230 - ETSETB - Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering
Academic year: 2019
Degree: BACHELOR'S DEGREE IN TELECOMMUNICATIONS TECHNOLOGIES AND SERVICES ENGINEERING (Syllabus 2015). (Teaching unit Compulsory)
ECTS credits: 6
Teaching languages: Catalan

Teaching staff
Coordinator: Jimenez Serres, Vicente
Others: Dominguez Pumar, Manuel M.
Salazar Soler, Jorge
Bardes Llorensi, Daniel
Pol Fernandez, Clemente
Madrenas Boadas, Jordi

Degree competences to which the subject contributes

Transversal:
07 AAT N2. SELF-DIRECTED LEARNING - Level 2: Completing set tasks based on the guidelines set by lecturers. Devoting the time needed to complete each task, including personal contributions and expanding on the recommended information sources.

Teaching methodology
Lectures
Laboratory sessions
Team assignments (at home)
Individual work
Continuous assessment evaluation
Final assessment evaluation

Learning objectives of the subject
Programming, analysis and design of microprocessor / microcontroller based systems.

Study load

<table>
<thead>
<tr>
<th>Total learning time: 150h</th>
<th>Hours large group:</th>
<th>39h</th>
<th>26.00%</th>
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<tbody>
<tr>
<td></td>
<td>Hours small group:</td>
<td>26h</td>
<td>17.33%</td>
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<tr>
<td></td>
<td>Self study:</td>
<td>85h</td>
<td>56.67%</td>
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## Content

<table>
<thead>
<tr>
<th>T1-Introduction</th>
<th>Learning time: 1h 58m</th>
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<tbody>
<tr>
<td></td>
<td>Theory classes: 1h</td>
</tr>
<tr>
<td></td>
<td>Self study: 0h 58m</td>
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</tbody>
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**Description:**
Subject description. Digital electronics context. Digital implementation options. Basic CPU system structure. Software execution.

<table>
<thead>
<tr>
<th>T2-Compilation and debugging</th>
<th>Learning time: 5h 50m</th>
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<tbody>
<tr>
<td></td>
<td>Theory classes: 3h</td>
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<tr>
<td></td>
<td>Self study: 2h 50m</td>
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**Description:**

<table>
<thead>
<tr>
<th>T3-Electrical compatibility</th>
<th>Learning time: 14h 28m</th>
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<tbody>
<tr>
<td></td>
<td>Theory classes: 5h</td>
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<tr>
<td></td>
<td>Self study: 9h 28m</td>
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**Description:**

<table>
<thead>
<tr>
<th>T4-The CPU</th>
<th>Learning time: 13h 36m</th>
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<tbody>
<tr>
<td></td>
<td>Theory classes: 7h</td>
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<tr>
<td></td>
<td>Self study: 6h 36m</td>
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**Description:**
### T5-Memory subsystem

**Description:**
Memory classification. Typical SRAM and ROM signals. Decoding. DRAM memories and others.

**Learning time:** 14h 28m  
Theory classes: 5h  
Self study: 9h 28m

### T6-Timing

**Description:**
content english

**Specific objectives:**
Requirements to evaluate. Timing and read/write evaluation. DRAM timing.

**Learning time:** 14h 28m  
Theory classes: 5h  
Self study: 9h 28m

### T7-Input/Output

**Description:**

**Learning time:** 11h 40m  
Theory classes: 6h  
Self study: 5h 40m

### T8-Programming model

**Description:**

**Learning time:** 4h 20m  
Theory classes: 1h 30m  
Self study: 2h 50m
Laboratory

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<th>Description:</th>
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Learning time: 58h
- Laboratory classes: 26h
- Self study: 32h

Qualification system

50% Final exam
30% Laboratory sessions
20% Continuous assessment evaluation

Bibliography

Basic:


Complementary: