Course guides
230091 - DSBM - Systems Based on Microprocessors Design

Unit in charge: Barcelona School of Telecommunications Engineering  
Teaching unit: 710 - EEL - Department of Electronic Engineering.
Degree: BACHELOR'S DEGREE IN TELECOMMUNICATIONS TECHNOLOGIES AND SERVICES ENGINEERING (Syllabus 2015). (Compulsory subject).
Academic year: 2021  ECTS Credits: 6.0  Languages: Catalan

LECTURER

Coordinating lecturer: Jimenez Serres, Vicente
Others: Dominguez Pumar, Manuel M.  
Salazar Soler, Jorge  
Bardes Llorensi, Daniel  
Pol Fernandez, Clemente  
Madrenas Boadas, Jordi

DEGREE COMPETENCES TO WHICH THE SUBJECT CONtributes

Transversal:
07 AAT N2. SELF-DIRECTED LEARNING - Level 2: Completing set tasks based on the guidelines set by lecturers. Devoting the time needed to complete each task, including personal contributions and expanding on the recommended information sources.

TEACHING METHODOLOGY

Lectures  
Laboratory sessions  
Team assignments (at home)  
Individual work  
Continuous assessment evaluation  
Final assessment evaluation

LEARNING OBJECTIVES OF THE SUBJECT

Programming, analysis and design of microprocessor / microcontroller based systems.

STUDY LOAD

<table>
<thead>
<tr>
<th>Type</th>
<th>Hours</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Self study</td>
<td>85,0</td>
<td>56.67</td>
</tr>
<tr>
<td>Hours large group</td>
<td>39,0</td>
<td>26.00</td>
</tr>
<tr>
<td>Hours small group</td>
<td>26,0</td>
<td>17.33</td>
</tr>
</tbody>
</table>

Total learning time: 150 h
## CONTENTS

### T1-Introduction

**Description:** Subject description. Digital electronics context. Digital implementation options. Basic CPU system structure. Software execution.

**Full-or-part-time:** 1h 58m  
Theory classes: 1h  
Self study : 0h 58m

### T2-Compilation and debugging


**Full-or-part-time:** 5h 50m  
Theory classes: 3h  
Self study : 2h 50m

### T3-Electrical compatibility

**Description:** Static and dynamic characteristics. Requirements and performance parameters. Compatibility in interconnections. Buses. Usage of open collector/drain in busses.

**Full-or-part-time:** 14h 28m  
Theory classes: 5h  
Self study : 9h 28m

### T4-The CPU


**Full-or-part-time:** 13h 36m  
Theory classes: 7h  
Self study : 6h 36m

### T5-Memory subsystem

**Description:** Memory classification. Typical SRAM and ROM signals. Decoding. DRAM memories and others.

**Full-or-part-time:** 14h 28m  
Theory classes: 5h  
Self study : 9h 28m
T6-Timing

**Description:**
content english

**Specific objectives:**
Requirements to evaluate. Timing and read/write evaluation. DRAM timing.

**Full-or-part-time:** 14h 28m
Theory classes: 5h
Self study : 9h 28m

T7-Input/Output

**Description:**

**Full-or-part-time:** 11h 40m
Theory classes: 6h
Self study : 5h 40m

T8-Programming model

**Description:**

**Full-or-part-time:** 4h 20m
Theory classes: 1h 30m
Self study : 2h 50m

Laboratory

**Description:**

**Full-or-part-time:** 58h
Laboratory classes: 26h
Self study : 32h

GRADING SYSTEM

50% Final exam
30% Laboratory sessions
20% Continuous assessment evaluation
BIBLIOGRAPHY

Basic:

Complementary: