Course guide
230091 - DSBM - Systems Based on Microprocessors Design

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.
Degree: BACHELOR'S DEGREE IN TELECOMMUNICATIONS TECHNOLOGIES AND SERVICES ENGINEERING (Syllabus 2015). (Compulsory subject).

Academic year: 2022  ECTS Credits: 6.0  Languages: Catalan

LECTURER

Coordinating lecturer: Consultar aquí / See here:
https://telecos.upc.edu/ca/estudis/curs-actual/professorat-responsables-coordinadors/responsables-assignatura

Others: Consultar aquí / See here:
https://telecos.upc.edu/ca/estudis/curs-actual/professorat-responsables-coordinadors/professorat-assignat-idioma

PRIOR SKILLS

Basic analysis of electronic circuits.
Basic knowledge of digital electronics.
Knowledge of C programming.

REQUIREMENTS

DIGITAL DESIGN - Precorequisite

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Transversal:
07 AAT N2. SELF-DIRECTED LEARNING - Level 2: Completing set tasks based on the guidelines set by lecturers. Devoting the time needed to complete each task, including personal contributions and expanding on the recommended information sources.

TEACHING METHODOLOGY

Lectures
Laboratory sessions
Team assignments (at home)
Individual work
Continuous assessment evaluation
Final assessment evaluation

LEARNING OBJECTIVES OF THE SUBJECT

Programming, analysis and design of microprocessor / microcontroller based systems.
STUDY LOAD

<table>
<thead>
<tr>
<th>Type</th>
<th>Hours</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Self study</td>
<td>85,0</td>
<td>56.67</td>
</tr>
<tr>
<td>Hours large group</td>
<td>39,0</td>
<td>26.00</td>
</tr>
<tr>
<td>Hours small group</td>
<td>26,0</td>
<td>17.33</td>
</tr>
</tbody>
</table>

Total learning time: 150 h

CONTENTS

T1-Introduction

Description:
Subject description. Digital electronics context. Digital implementation options. Basic CPU system structure. Software execution.

Full-or-part-time: 1h 58m
Theory classes: 1h
Self study : 0h 58m

T2-Compilation and debugging

Description:

Full-or-part-time: 5h 50m
Theory classes: 3h
Self study : 2h 50m

T3-Electrical compatibility

Description:

Full-or-part-time: 14h 28m
Theory classes: 5h
Self study : 9h 28m

T4-The CPU

Description:

Full-or-part-time: 13h 36m
Theory classes: 7h
Self study : 6h 36m
<table>
<thead>
<tr>
<th>Topic</th>
<th>Description</th>
<th>Specific objectives</th>
<th>Full-or-part-time:</th>
<th>Theory classes:</th>
<th>Self study:</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>T5-Memory subsystem</strong></td>
<td>Memory classification. Typical SRAM and ROM signals. Decoding. DRAM memories and others.</td>
<td>Requirements to evaluate. Timing and read/write evaluation. DRAM timing.</td>
<td>14h 28m</td>
<td>5h</td>
<td>9h 28m</td>
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<tr>
<td><strong>T6-Timing</strong></td>
<td>content english</td>
<td></td>
<td>14h 28m</td>
<td>5h</td>
<td>9h 28m</td>
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<tr>
<td><strong>T7-Input/Output</strong></td>
<td>Peripheral connections. I/O map. Registers. Polling and interrupt synchronization. RSIs. Execution context. Masking. Latency. Exceptions. Peripheral examples: Timers, Converters, Communications.</td>
<td></td>
<td>11h 40m</td>
<td>6h</td>
<td>5h 40m</td>
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<tr>
<td><strong>T8-Programming model</strong></td>
<td>Tasks and events. CPU usage. Operating systems. Processes. Real time systems. Scheduling. Process synchronization.</td>
<td></td>
<td>4h 20m</td>
<td>1h 30m</td>
<td>2h 50m</td>
</tr>
<tr>
<td><strong>Laboratory</strong></td>
<td>ARM Cortex M4 system development. Development environment. Peripheral access. Interrupts. Timing measurements. Threads.</td>
<td></td>
<td>58h</td>
<td>26h</td>
<td>32h</td>
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GRADING SYSTEM

50% Final exam
30% Laboratory sessions
20% Continuous assessment evaluation

In the reassessment exam, only the theory contents are reassessed, so the resulting grade from the reassessment will be:

70% Reassessment Exam
30% Previous laboratory work

BIBLIOGRAPHY

Basic:

Complementary: