Last update: 05-07-2019

230114 - DSP-FPGA - Real-Time Dsp System Design with Fpga

Coordinating unit: 230 - ETSETB - Barcelona School of Telecommunications Engineering

Teaching unit: 710 - EEL - Department of Electronic Engineering

Academic year: 2019

Degree: BACHELOR'S DEGREE IN ELECTRONIC SYSTEMS ENGINEERING (Syllabus 2009). (Teaching unit Optional)
BACHELOR'S DEGREE IN TELECOMMUNICATIONS SCIENCE AND TECHNOLOGY (Syllabus 2010). (Teaching unit Optional)
BACHELOR'S DEGREE IN AUDIOVISUAL SYSTEMS ENGINEERING (Syllabus 2009). (Teaching unit Optional)
BACHELOR'S DEGREE IN TELECOMMUNICATIONS SYSTEMS ENGINEERING (Syllabus 2010). (Teaching unit Optional)
BACHELOR'S DEGREE IN TELECOMMUNICATIONS TECHNOLOGIES AND SERVICES ENGINEERING (Syllabus 2015). (Teaching unit Optional)

ECTS credits: 6 Teaching languages: English

Teaching staff

Coordinator: JORDI MADRENAS

Others: JORDI MADRENAS

Prior skills

Basic digital signal processing, Digital design, VHDL or Verilog description, (Micro)processor Systems, Basic computer programming.

Teaching methodology

- Lectures
- Laboratory classes
- Group work (distance)
- Individual work (distance)
- Short answer test (Control)
- Short answer test (Test)
- Extended answer test (Final Exam)

Learning objectives of the subject

- To acquire a methodology for fast and efficient implementation of DSP algorithms on FPGAs.
- To decide the partition between software and hardware in order to obtain the higher efficiency.
- To design hardware considering the tradeoff between area, performance and power consumption, depending on the application.
- To use of CAE tools available for mapping DSP algorithms on FPGAs.
- To implement physical DSP algorithms on real FPGAs.

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Study load

Total learning time: 150h	Hours large group:	26h	17.33%
	Hours small group:	26h	17.33%
	Self study:	98h	65.33%

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Content

1. Introduction to real-time digital signal processing (DSP)

Learning time: 12h
Theory classes: 6h
Self study : 6h

Description:
The DSP algorithms requirements as well as demanded resources for real-time performance are analyzed. Several DSP algorithms are reviewed, with emphasis on image processing.

2. DSP algorithm description with high level languages

Learning time: 18h
Theory classes: 4h
Laboratory classes: 4h
Self study : 10h

Description:
Matlab/Simulink environament for DSP algorithm description.

3. FPGA Architectures

Learning time: 24h
Theory classes: 6h
Laboratory classes: 4h
Self study : 14h

Description:
Introduction to the main FPGA architectures with emphasis on DSP blocs and IP cores. Introduction to the Xilinx development environment.

4. Algorithm mapping for real-time digital signal processing (DSP)

Learning time: 42h
Theory classes: 10h
Laboratory classes: 8h
Self study : 24h

Description:
Introduction to the DSP system hardware implementation concepts. Implementation and transformation forms: serial and parallel processing (in space and time), retiming, etc.. Analysis of DSP algorithm mapping on programmable hardware and area/delay/power consumption tradeoffs. Study of the finite precision effect. Fixed and floating point. Automatic generation tools (System Generator).

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5. Design project on development boards	Learning time: 54h Laboratory classes: 10h Self study : 44h

Description:
Design of a project on advanced development boards of Xilinx 7 family or Zynq.

Planning of activities

LABORATORY

Description:
Labs on DSP algorithm description using Matlab/Simulink, mapping and implementation on FPGA with ISE and System Generator. Design project on real-time processing, with emphasis on image processing.

SHORT ANSWER TEST (CONTROL)

Description:
Mid-term exam.

EXTENDED ANSWER TEST (FINAL EXAMINATION)

Description:
Final exam.

Qualification system

The final grade will be obtained from the continuous assessment qualification (works proposed by the lecturer throughout the course and laboratory practices) and the final exam, according to the following criteria:
Laboratory assessments: 70%
Partial examinations and controls: 10%
Final examination: 20%

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Bibliography

Basic:

Bailey, D.G. Design for embedded image processing on FPGAs [on line]. Singapore: Wiley & Soncs, 2011 [Consultation: 07/10/2014]. Available on: <http://onlinelibrary.wiley.com/book/10.1002/9780470828519>. ISBN 9780470828496.

Khan, S. Digital design of signal processing systems: a practical approach [on line]. Chichester: Wiley & Sons, 2011 [Consultation: 07/10/2014]. Available on: <http://onlinelibrary.wiley.com/book/10.1002/9780470974681>. ISBN 9780470741832.

Others resources:

Matlab, Simulink, System Generator and ISE User guides.