Course guides
230114 - DSP-FPGA - Real-Time Dsp System Design with Fpga

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree:
- BACHELOR’S DEGREE IN AUDIOVISUAL SYSTEMS ENGINEERING (Syllabus 2009). (Optional subject).
- BACHELOR’S DEGREE IN ELECTRONIC SYSTEMS ENGINEERING (Syllabus 2009). (Optional subject).
- BACHELOR’S DEGREE IN TELECOMMUNICATIONS SCIENCE AND TECHNOLOGY (Syllabus 2010). (Optional subject).
- BACHELOR’S DEGREE IN TELECOMMUNICATIONS SYSTEMS ENGINEERING (Syllabus 2010). (Optional subject).
- BACHELOR’S DEGREE IN TELECOMMUNICATIONS TECHNOLOGIES AND SERVICES ENGINEERING (Syllabus 2015). (Optional subject).
- BACHELOR’S DEGREE IN ELECTRONIC ENGINEERING AND TELECOMMUNICATION (Syllabus 2018). (Optional subject).

Academic year: 2021  ECTS Credits: 6.0  Languages: English

LECTURER
Coordinating lecturer: JORDI MADRENAS
Others: JORDI MADRENAS

PRIOR SKILLS
Basic digital signal processing, Digital design, VHDL or Verilog description, (Micro)processor Systems, Basic computer programming.

TEACHING METHODOLOGY
- Lectures
- Laboratory classes
- Group work (distance)
- Individual work (distance)
- Short answer test (Control)
- Short answer test (Test)
- Extended answer test (Final Exam)

LEARNING OBJECTIVES OF THE SUBJECT
- To acquire a methodology for fast and efficient implementation of DSP algorithms on FPGAs.
- To decide the partition between software and hardware in order to obtain the higher efficiency.
- To design hardware considering the tradeoff between area, performance and power consumption, depending on the application.
- To use of CAE tools available for mapping DSP algorithms on FPGAs.
- To implement physical DSP algorithms on real FPGAs.
STUDY LOAD

<table>
<thead>
<tr>
<th>Type</th>
<th>Hours</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>Hours large group</td>
<td>26,0</td>
<td>17.33</td>
</tr>
<tr>
<td>Self study</td>
<td>98,0</td>
<td>65.33</td>
</tr>
<tr>
<td>Hours small group</td>
<td>26,0</td>
<td>17.33</td>
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</tbody>
</table>

Total learning time: 150 h

CONTENTS

1. Introduction to real-time digital signal processing (DSP)
   Description:
The DSP algorithms requirements as well as demanded resources for real-time performance are analyzed. Several DSP algorithms are reviewed, with emphasis on image processing.
   Full-or-part-time: 12h
   Theory classes: 6h
   Self study: 6h

2. DSP algorithm description with high level languages
   Description:
   Matlab/Simulink environment for DSP algorithm description.
   Full-or-part-time: 18h
   Theory classes: 4h
   Laboratory classes: 4h
   Self study: 10h

3. FPGA Architectures
   Description:
   Introduction to the main FPGA architectures with emphasis on DSP blocs and IP cores. Introduction to the Xilinx development environment.
   Full-or-part-time: 24h
   Theory classes: 6h
   Laboratory classes: 4h
   Self study: 14h
4. Algorithm mapping for real-time digital signal processing (DSP)

Description:
Introduction to the DSP system hardware implementation concepts. Implementation and transformation forms: serial and parallel processing (in space and time), retiming, etc. Analysis of DSP algorithm mapping on programmable hardware and area/delay/power consumption tradeoffs. Study of the finite precision effect. Fixed and floating point. Automatic generation tools (System Generator).

Full-or-part-time: 42h
Theory classes: 10h
Laboratory classes: 8h
Self study: 24h

5. Design project on development boards

Description:
Design of a project on advanced development boards of Xilinx 7 family or Zynq.

Full-or-part-time: 54h
Laboratory classes: 10h
Self study: 44h

ACTIVITIES

LABORATORY

Description:
Labs on DSP algorithm description using Matlab/Simulink, mapping and implementation on FPGA with ISE and System Generator. Design project on real-time processing, with emphasis on image processing.

SHORT ANSWER TEST (CONTROL)

Description:
Mid-term exam.

EXTENDED ANSWER TEST (FINAL EXAMINATION)

Description:
Final exam.

GRADING SYSTEM

The final grade will be obtained from the continuous assessment qualification (works proposed by the lecturer throughout the course and laboratory practices) and the final exam, according to the following criteria:
Laboratory assessments: 70%
Partial examinations and controls: 10%
Final examination: 20%
BIBLIOGRAPHY

Basic:

RESOURCES

Other resources:
Matlab, Simulink, System Generator and ISE User guides.