230114 - DSP-FPGA - Real-Time Dsp System Design with Fpga

Coordinating unit: 230 - ETSETB - Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering
Academic year: 2019
Degree: BACHELOR'S DEGREE IN ELECTRONIC SYSTEMS ENGINEERING (Syllabus 2009). (Teaching unit Optional)
BACHELOR'S DEGREE IN TELECOMMUNICATIONS SCIENCE AND TECHNOLOGY (Syllabus 2010). (Teaching unit Optional)
BACHELOR'S DEGREE IN AUDIOVISUAL SYSTEMS ENGINEERING (Syllabus 2009). (Teaching unit Optional)
BACHELOR'S DEGREE IN TELECOMMUNICATIONS SYSTEMS ENGINEERING (Syllabus 2010). (Teaching unit Optional)
BACHELOR'S DEGREE IN TELECOMMUNICATIONS TECHNOLOGIES AND SERVICES ENGINEERING (Syllabus 2015). (Teaching unit Optional)
ECTS credits: 6
Teaching languages: English

Teaching staff
Coordinator: JORDI MADRENAS
Others: JORDI MADRENAS

Prior skills
Basic digital signal processing, Digital design, VHDL or Verilog description, (Micro)processor Systems, Basic computer programming.

Teaching methodology
- Lectures
- Laboratory classes
- Group work (distance)
- Individual work (distance)
- Short answer test (Control)
- Short answer test (Test)
- Extended answer test (Final Exam)

Learning objectives of the subject
- To acquire a methodology for fast and efficient implementation of DSP algorithms on FPGAs.
- To decide the partition between software and hardware in order to obtain the higher efficiency.
- To design hardware considering the tradeoff between area, performance and power consumption, depending on the application.
- To use of CAE tools available for mapping DSP algorithms on FPGAs.
- To implement physical DSP algorithms on real FPGAs.
## Study load

<table>
<thead>
<tr>
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<th>Hours large group:</th>
<th>%</th>
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<tbody>
<tr>
<td>Total learning time</td>
<td>150h</td>
<td>17.33%</td>
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<td>Hours small group:</td>
<td>26h</td>
<td>17.33%</td>
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<tr>
<td>Self study:</td>
<td>98h</td>
<td>65.33%</td>
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## Content

<table>
<thead>
<tr>
<th>Chapter</th>
<th>Title</th>
<th>Learning Time</th>
<th>Description</th>
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<tbody>
<tr>
<td><strong>1.</strong></td>
<td><strong>Introduction to real-time digital signal processing (DSP)</strong></td>
<td><strong>12h</strong></td>
<td><strong>Theory classes: 6h</strong>&lt;br&gt;<strong>Self study: 6h</strong>&lt;br&gt;&lt;br&gt;&lt;br&gt;<strong>Description:</strong>&lt;br&gt;The DSP algorithms requirements as well as demanded resources for real-time performance are analyzed. Several DSP algorithms are reviewed, with emphasis on image processing.</td>
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<td><strong>2.</strong></td>
<td><strong>DSP algorithm description with high level languages</strong></td>
<td><strong>18h</strong></td>
<td><strong>Theory classes: 4h</strong>&lt;br&gt;<strong>Laboratory classes: 4h</strong>&lt;br&gt;<strong>Self study: 10h</strong>&lt;br&gt;&lt;br&gt;&lt;br&gt;<strong>Description:</strong>&lt;br&gt;MATLAB/Simulink environment for DSP algorithm description.</td>
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<td><strong>3.</strong></td>
<td><strong>FPGA Architectures</strong></td>
<td><strong>24h</strong></td>
<td><strong>Theory classes: 6h</strong>&lt;br&gt;<strong>Laboratory classes: 4h</strong>&lt;br&gt;<strong>Self study: 14h</strong>&lt;br&gt;&lt;br&gt;&lt;br&gt;<strong>Description:</strong>&lt;br&gt;Introduction to the main FPGA architectures with emphasis on DSP blocks and IP cores. Introduction to the Xilinx development environment.</td>
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<td><strong>4.</strong></td>
<td><strong>Algorithm mapping for real-time digital signal processing (DSP)</strong></td>
<td><strong>42h</strong></td>
<td><strong>Theory classes: 10h</strong>&lt;br&gt;<strong>Laboratory classes: 8h</strong>&lt;br&gt;<strong>Self study: 24h</strong>&lt;br&gt;&lt;br&gt;&lt;br&gt;<strong>Description:</strong>&lt;br&gt;Introduction to the DSP system hardware implementation concepts. Implementation and transformation forms: serial and parallel processing (in space and time), retiming, etc.. Analysis of DSP algorithm mapping on programmable hardware and area/delay/power consumption tradeoffs. Study of the finite precision effect. Fixed and floating point. Automatic generation tools (System Generator).</td>
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Planning of activities

LABORATORY

Description:
Labs on DSP algorithm description using Matlab/Simulink, mapping and implementation on FPGA with ISE and System Generator. Design project on real-time processing, with emphasis on image processing.

SHORT ANSWER TEST (CONTROL)

Description:
Mid-term exam.

EXTENDED ANSWER TEST (FINAL EXAMINATION)

Description:
Final exam.

Qualification system

The final grade will be obtained from the continuous assessment qualification (works proposed by the lecturer throughout the course and laboratory practices) and the final exam, according to the following criteria:
Laboratory assessments: 70%
Partial examinations and controls: 10%
Final examination: 20%
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Bibliography

Basic:


Others resources:

Matlab, Simulink, System Generator and ISE User guides.