Learning objectives of the subject

- To acquire a methodology for fast and efficient implementation of DSP algorithms on FPGAs.
- To decide the partition between software and hardware in order to obtain the higher efficiency.
- To design hardware considering the tradeoff between area, performance and power consumption, depending on the application.
- To use of CAE tools available for mapping DSP algorithms on FPGAs.
- To implement physical DSP algorithms on real FPGAs.
## Study load

<table>
<thead>
<tr>
<th>Total learning time: 150h</th>
<th>Hours large group: 26h</th>
<th>17.33%</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Hours small group: 26h</td>
<td>17.33%</td>
</tr>
<tr>
<td></td>
<td>Self study: 98h</td>
<td>65.33%</td>
</tr>
</tbody>
</table>
## 1. Introduction to real-time digital signal processing (DSP)

**Description:**
The DSP algorithms requirements as well as demanded resources for real-time performance are analyzed. Several DSP algorithms are reviewed, with emphasis on image processing.

**Learning time:** 12h  
Theory classes: 6h  
Self study: 6h

## 2. DSP algorithm description with high level languages

**Description:**
Matlab/Simulink environment for DSP algorithm description.

**Learning time:** 18h  
Theory classes: 4h  
Laboratory classes: 4h  
Self study: 10h

## 3. FPGA Architectures

**Description:**
Introduction to the main FPGA architectures with emphasis on DSP blocks and IP cores. Introduction to the Xilinx development environment.

**Learning time:** 24h  
Theory classes: 6h  
Laboratory classes: 4h  
Self study: 14h

## 4. Algorithm mapping for real-time digital signal processing (DSP)

**Description:**
Introduction to the DSP system hardware implementation concepts. Implementation and transformation forms: serial and parallel processing (in space and time), retiming, etc. Analysis of DSP algorithm mapping on programmable hardware and area/delay/power consumption tradeoffs. Study of the finite precision effect. Fixed and floating point. Automatic generation tools (System Generator).

**Learning time:** 42h  
Theory classes: 10h  
Laboratory classes: 8h  
Self study: 24h
5. Design project on development boards

**Description:**
Design of a project on advanced development boards of Xilinx 7 family or Zynq.

**Learning time:** 54h
- Laboratory classes: 10h
- Self study: 44h

### Planning of activities

**LABORATORY**

**Description:**
Labs on DSP algorithm description using Matlab/Simulink, mapping and implementation on FPGA with ISE and System Generator. Design project on real-time processing, with emphasis on image processing.

**SHORT ANSWER TEST (CONTROL)**

**Description:**
Mid-term exam.

**EXTENDED ANSWER TEST (FINAL EXAMINATION)**

**Description:**
Final exam.

### Qualification system

- Final examination: 20%
- Partial examinations and controls: 10%
- Laboratory assessments: 70%

### Bibliography

**Basic:**

**Others resources:**
- Matlab, Simulink, System Generator and ISE User guides.