Degree competences to which the subject contributes

Transversal:

07 AAT N3. SELF-DIRECTED LEARNING - Level 3. Applying the knowledge gained in completing a task according to its relevance and importance. Deciding how to carry out a task, the amount of time to be devoted to it and the most suitable information sources.

Teaching methodology

Lectures: presentations on each specific topic and collective analysis of cases of electronic digital design.
Classes of problems: Study of digital design problems related to exposed theory.
Laboratory classes: Design, analysis and development of digital circuitry associated with the exposed theory and telecommunications. These laboratory activities will be implemented in Terasic development boards using ALTERA programmable devices.
Short-answer tests (controls) and extended-response (final exam)

Learning objectives of the subject

The main objective will be the design of synchronous circuits of medium and high complexity for applications preferably communications and signal processing in real time.
Rapid prototyping is the focus of the subject. Implement efficient designs require good training in the hardware
description language VHDL, knowledge and use of design tools, architectures of FPGAs, as well as advanced digital design concepts.

The study and characterization of features, especially the temporal behavior of designs will also be important. Knowing the physical limitations of the devices is a priority to calculate the basic parameters of the circuits: maximum operating frequency, power dissipation, cost and occupied area.

Assimilation and consolidation of knowledge will be achieve implementing the designs in the laboratory with design tools and commercial devices.

List of specific objectives of the course:
* The use of methodologies and design tools for complex sequential digital systems.
* To analyze some of the issues of greatest impact in the digital design.
* Identify and evaluate alternative implementation of digital systems, including programmable logic devices.
* Understanding and using hardware description languages, including VHDL.

### Study load

<table>
<thead>
<tr>
<th>Total learning time: 149h</th>
<th>Hours large group:</th>
<th>26h</th>
<th>17.45%</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Hours small group:</td>
<td>26h</td>
<td>17.45%</td>
</tr>
<tr>
<td></td>
<td>Self study:</td>
<td>97h</td>
<td>65.10%</td>
</tr>
</tbody>
</table>
# Content

## 1. Design of digital electronic systems

<table>
<thead>
<tr>
<th>Description</th>
<th>Learning time: 37h</th>
</tr>
</thead>
</table>
| 1.1. Design strategies.  
1.2. Programmable logic devices: CPLDs, FPGAs.  
1.3. Rapid prototyping tools.  
1.3.1. Hardware description languages, types and levels of description.  
1.3.2. Synthesis.  
1.3.3. Simulation. Timing constraints and performance verification.  
1.3.4. Guidelines for manufacturing test. | Theory classes: 6h 30m  
Laboratory classes: 6h 30m  
Self study: 24h |

## 2. Synthesis with VHDL

<table>
<thead>
<tr>
<th>Description</th>
<th>Learning time: 37h</th>
</tr>
</thead>
</table>
| 2.1. Reminder of the main features.  
2.2. Libraries.  
2.3. Functions and procedures.  
2.4. Inference of specific blocks.  
2.4.1. Generation and distribution of clock signals.  
2.4.2. Arithmetic blocks.  
2.4.3. Memory blocks. Implementation of stacks. | Theory classes: 6h 30m  
Laboratory classes: 6h 30m  
Self study: 24h |

## 3. Design techniques

<table>
<thead>
<tr>
<th>Description</th>
<th>Learning time: 37h</th>
</tr>
</thead>
</table>
| 3.1. Concurrent state machines.  
3.2. Algorithmic machines.  
3.2.1. Data subsystem. Pipelining.  
3.2.2. Control subsystem.  
3.2.3. Microprogrammable systems.  
3.3. Methods to reduce consumption.  
3.4. Structures and standards of test.  
3.5. IP cores. | Theory classes: 6h 30m  
Laboratory classes: 6h 30m  
Self study: 24h |

<table>
<thead>
<tr>
<th>Learning time: 37h</th>
</tr>
</thead>
<tbody>
<tr>
<td>Theory classes: 6h 30m</td>
</tr>
<tr>
<td>Laboratory classes: 6h 30m</td>
</tr>
<tr>
<td>Self study : 24h</td>
</tr>
</tbody>
</table>

**Description:**
4.1.1. Temporal analysis.
4.1.2. Metastability.
4.1.3. Hazards.
4.1.4. Synchronous versus asynchronous.
4.2. Synthesis of frequency.
4.3. Interface with memories and other peripherals.
4.4. Test.

**Qualification system**

Continuous theory assessment: controls, exercises and / or works to be done during the course (CT)
Final theory exam (FTE)
Final theory grade of (FTG): Maximum (FTE , 0.5FTE + 0.5CT)
Continuous laboratory assessment (CL): Activity Tracking
Final Laboratory exam (FLE)
Final Laboratory grade (NLG): 0.75CL + 0.25 FLE
Final note subject = 0.5FTG + 0.5 NLG

**Regulations for carrying out activities**

Exams: Individual
Individual work: Individual
Laboratory groups: maximum two students
Bibliography

Basic:


