Last update: 06-05-2019

230120 - DSED - Design of Digital Electronic Systems

Coordinating unit: 230 - ETSETB - Barcelona School of Telecommunications Engineering

Teaching unit: 710 - EEL - Department of Electronic Engineering

Academic year: 2019

Degree: BACHELOR'S DEGREE IN TELECOMMUNICATIONS TECHNOLOGIES AND SERVICES ENGINEERING (Syllabus 2015). (Teaching unit Optional)

ECTS credits: 5 Teaching languages: Catalan, Spanish

Teaching staff

Coordinator: Chavez Dominguez, Juan Antonio
Rubio Sola, Jose Antonio

Others: Pons Nin, Joan
Moll Echeto, Francesc De Borja

Opening hours

Timetable: 6 hours of dedication each professor

Prior skills

Basic knowledge of CMOS technology.
Basic knowledge of combinational and sequential digital design.
Basic knowledge of microprocessor architectures.

Requirements

DISSENY DIGITAL - Precorequisit

Degree competences to which the subject contributes

Transversal:

07 AAT N3. SELF-DIRECTED LEARNING - Level 3. Applying the knowledge gained in completing a task according to its relevance and importance. Deciding how to carry out a task, the amount of time to be devoted to it and the most suitable information sources.

Teaching methodology

Lectures: presentations on each specific topic and collective analysis of cases of electronic digital design.
Classes of problems: Study of digital design problems related to exposed theory.
Laboratory classes: Design, analysis and development of digital circuitry associated with the exposed theory and telecommunications. These laboratory activities will be implemented in Terasic development boards using ALTERA programmable devices.
Short-answer tests (controls) and extended-response (final exam)

Learning objectives of the subject

The main objective will be the design of synchronous circuits of medium and high complexity for applications preferably communications and signal processing in real time.
Rapid prototyping is the focus of the subject. Implement efficient designs require good training in the hardware

230120 - DSED - Design of Digital Electronic Systems

description language VHDL, knowledge and use of design tools, architectures of FPGAs, as well as advanced digital design concepts.
The study and characterization of features, especially the temporal behavior of designs will also be important. Knowing the physical limitations of the devices is a priority to calculate the basic parameters of the circuits: maximum operating frequency, power dissipation, cost and occupied area.
Assimilation and consolidation of knowledge will be achieve implementing the designs in the laboratory with design tools and commercial devices.
List of specific objectives of the course:
* The use of methodologies and design tools for complex sequential digital systems.
* To analyze some of the issues of greatest impact in the digital design.
* Identify and evaluate alternative implementation of digital systems, including programmable logic devices.
* Understanding and using hardware description languages, including VHDL.

Study load

Total learning time: 149h	Hours large group:	26h	17.45%
	Hours small group:	26h	17.45%
	Self study:	97h	65.10%

Last update: 06-05-2019

230120 - DSED - Design of Digital Electronic Systems

Content

1. Design of digital electronic systems

Learning time: 37h

Theory classes: 6h 30m
Laboratory classes: 6h 30m
Self study : 24h

Description:
1.1. Design strategies.
1.2. Programmable logic devices: CPLDs, FPGAs.
1.3. Rapid prototyping tools.
1.3.1. Hardware description languages, types and levels of description.
1.3.2. Synthesis.
1.3.3. Simulation. Timing constraints and performance verification.
1.3.4. Guidelines for manufacturing test.

2. Synthesis with VHDL

Learning time: 37h

Theory classes: 6h 30m
Laboratory classes: 6h 30m
Self study : 24h

Description:
2.1. Reminder of the main features.
2.2. Libraries.
2.3. Functions and procedures.
2.4. Inference of specific blocks.
2.4.1. Generation and distribution of clock signals.
2.4.2. Arithmetic blocks.
2.4.3. Memory blocks. Implementation of stacks.

3. Design techniques

Learning time: 37h

Theory classes: 6h 30m
Laboratory classes: 6h 30m
Self study : 24h

Description:
3.1. Concurrent state machines.
3.2. Algorithmic machines.
3.2.1. Data subsystem. Pipelining.
3.2.2. Control subsystem.
3.2.3. Microprogrammable systems.
3.3. Methods to reduce consumption.
3.4. Structures and standards of test.
3.5. IP cores.

230120 - DSED - Design of Digital Electronic Systems

4. Design Issues.	Learning time: 37h Theory classes: 6h 30m Laboratory classes: 6h 30m Self study : 24h

Description:
4.1. Timing of digital circuits.
4.1.1. Temporal analysis.
4.1.2. Metastability.
4.1.3. Hazards.
4.1.4. Synchronous versus asynchronous.
4.2. Synthesis of frequency.
4.3. Interface with memories and other peripherals.
4.4. Test.

Qualification system

Continuous theory assessment: controls, exercises and / or works to be done during the course (CT)
Final theory exam (FTE)
Final theory grade of (FTG): Maximum (FTE , 0.5FTE + 0.5CT)
Continuous laboratory assessment (CL): Activity Tracking
Final Laboratory exam (FLE)
Final Laboratory grade (NLG): 0.75CL + 0.25 FLE
Final note subject = 0.5FTG + 0.5 NLG

Regulations for carrying out activities

Exams: Individual
Individual work: Individual
Laboratory groups: maximum two students

Last update: 06-05-2019

230120 - DSED - Design of Digital Electronic Systems

Bibliography

Basic:

Gajski, Daniel D. Principles of digital design. Upper Saddle River, N.J: Prentice Hall, 1997. ISBN 0132423979.

Brown, S.D.; Vranesic, Z. Fundamentals of digital logic with VHDL design. 3rd ed. Boston [etc.]: McGraw-Hill, 2009. ISBN 9780071268806.

Skahill, Kevin. VHDL for PROGRAMMABLE LOGIC. 2006. Reading [etc.]: Addison Wesley, 1996. ISBN 0201895730.

Harris, S.L. ; Money, D. Digital design and computer architecture. ARM ed. Waltham, MA: Morgan Kaufmann, 2016. ISBN 9780128000564.

Ashenden, P. J. The Designer's guide to VHDL [on line]. 3rd ed. Burlington: Morgan Kaufmann, 2008 [Consultation: 14/06/2017]. Available on: <http://www.sciencedirect.com/science/book/9780120887859>. ISBN 9780120887859.

Scarpino, Frank. VHDL and AHDL Digital System Implementation. Prentice Hall, 1998. ISBN 9780138570873.

Ashenden, P. J. The VHDL cookbook [on line]. Adelaide, S. Aust.: Dept. of Computer Science, University of Adelaide, 1991 [Consultation: 15/06/2017]. Available on: <https://pdfs.semanticscholar.org/75a1/318163592901aaa5a83728615979bba13707.pdf>.