Course guides
230921 - SDC - Configurable Digital Systems

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.
Degree: BACHELOR'S DEGREE IN ELECTRONIC ENGINEERING AND TELECOMMUNICATION (Syllabus 2018).
(Compulsory subject).
Academic year: 2021  ECTS Credits: 6.0  Languages: Catalan

LECTURER

Coordinating lecturer: Joan Pons Nin
Juan Antonio Chávez Domínguez

Others: Joan Pons Nin
Juan Antonio Chávez Domínguez

PRIOR SKILLS

Basic knowledge of CMOS technology.
Basic knowledge of combinational and sequential digital design.
Basic knowledge of microprocessor architectures.

REQUIREMENTS

DISSENY DIGITAL (2A)

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
CE15. (ENG) GREELEC: Coneixement i aplicació dels fonamentals llenguatges de descripció de dispositius de hardware. (Mòdul comú a la branca de telecomunicació).
CE24. (ENG) GREELEC: Capacitat per aplicar l'electrònica com tecnologia de suport a altres camps i activitats, i no només en l'àmbit de les tecnologies de la informació i comunicació. (Mòdul de tecnologia específica- Sistemes electrònics).
CE27. (ENG) GREELEC: Capacitat per a dissenyar dispositius d'interfície, captura de dades i emmagatzament, i terminals per serveis i sistemes de telecomunicació. (Mòdul de tecnologia específica- Sistemes electrònics).

Transversal:
CT4. (ENG) GREELEC: TREBALL EN EQUIP: ser caça de treballar com a membre d'un equip interdisciplinari, ja sigui com un membre més o realitzant tasques de direcció, amb la finalitat de continuar a desenvolupar projectes amb pragmatisme i sentit de la responsabilitat, assumint compromisos tenint en compte els recursos disponibles.

Basic:
CB4. (ENG) GREELEC: Que els estudiants puguin transmetre informació, idees, problemes i solucions a un públic tant especialitzat com no especialitzat.
TEACHING METHODOLOGY

Lectures: presentations on each specific topic and collective analysis of cases of electronic digital design.
Classes of problems: Study of digital design problems related to exposed theory.
Laboratory classes: Design, analysis and development of digital circuitry associated with the exposed theory and realistic applications. These laboratory activities will be implemented in test & development boards using Xilinx programmable devices.
Short-answer tests (controls) and extended-response (final exam)

LEARNING OBJECTIVES OF THE SUBJECT

The main objective will be the design of synchronous circuits of medium and high complexity for applications preferably communications and signal processing in real time.
Rapid prototyping is the focus of the subject. Implement efficient designs require good training in the hardware description language VHDL, knowledge and use of design tools, architectures of FPGAs, as well as advanced digital design concepts.
The study and characterization of features, especially the temporal behavior of designs will also be important. Knowing the physical limitations of the devices is a priority to calculate the basic parameters of the circuits: maximum operating frequency, power dissipation, cost and occupied area.
Assimilation and consolidation of knowledge will be achieve implementing the designs in the laboratory with design tools and commercial devices.
List of specific objectives of the course:
* The use of methodologies and design tools for complex sequential digital systems.
* To analyze some of the issues of greatest impact in the digital design.
* Identify and evaluate alternative implementation of digital systems, including programmable logic devices.
* Understanding and using hardware description languages, including VHDL.

STUDY LOAD

<table>
<thead>
<tr>
<th>Type</th>
<th>Hours</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>Hours large group</td>
<td>39,0</td>
<td>26.00</td>
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<tr>
<td>Self study</td>
<td>85,0</td>
<td>56.67</td>
</tr>
<tr>
<td>Hours small group</td>
<td>26,0</td>
<td>17.33</td>
</tr>
</tbody>
</table>

Total learning time: 150 h

CONTENTS

Design of digital electronic systems

Description:
1.1. Design strategies.
1.2. Programmable logic devices: CPLDs, FPGAs.
1.3. Rapid prototyping tools.
1.3.1. Hardware description languages, types and levels of description.
1.3.2. Synthesis.
1.3.3. Simulation. Timing constraints and performance verification.
1.3.4. Guidelines for manufacturing test.

Full-or-part-time: 37h
Theory classes: 9h 45m
Laboratory classes: 6h 30m
Self study : 20h 45m
### Synthesis with VHDL

**Description:**
- 2.1. Reminder of the main features.
- 2.2. Libraries.
- 2.3. Functions and procedures.
- 2.4. Inference of specific blocks.
  - 2.4.1. Generation and distribution of clock signals.
  - 2.4.2. Arithmetic blocks.
  - 2.4.3. Memory blocks. Implementation of stacks.

**Full-or-part-time:** 37h  
Theory classes: 9h 45m  
Laboratory classes: 6h 30m  
Self study: 20h 45m

### Design techniques

**Description:**
- 3.2. Algorithmic machines.
  - 3.2.1. Data subsystem. Pipelining.
  - 3.2.2. Control subsystem.
- 3.3. Microprogrammable systems.
- 3.4. Methods to reduce consumption.
- 3.5. Structures and standards of test.

**Full-or-part-time:** 38h  
Theory classes: 9h 45m  
Laboratory classes: 6h 30m  
Self study: 21h 45m

### Design Issues

**Description:**
  - 4.1.1. Temporal analysis.
  - 4.1.2. Metastability.
  - 4.1.3. Hazards.
  - 4.1.4. Synchronous versus asynchronous.
- 4.2. Synthesis of frequency.
- 4.3. Interface with memories and other peripherals.
- 4.4. Test.

**Full-or-part-time:** 38h  
Theory classes: 9h 45m  
Laboratory classes: 6h 30m  
Self study: 21h 45m
GRADING SYSTEM

Continuous theory assessment: controls, exercises and / or works to be done during the course (CT)
Final theory exam (FTE)
Final theory grade of (FTG): Maximum (FTE , 0.5FTE + 0.5CT)
Continuous laboratory assessment (CL): Activity Tracking
Final Laboratory exam (FLE)
Final Laboratory grade (NLG): 0.75CL + 0.25 FLE
Final note subject = 0.5FTG + 0.5 NLG

EXAMINATION RULES.

Exams: Individual
Individual work: Individual
Laboratory groups: maximum two students

BIBLIOGRAPHY

Basic: