270060 - AC2 - Computer Architecture II

Coordinating unit: 270 - FIB - Barcelona School of Informatics
Teaching unit: 701 - AC - Department of Computer Architecture
Academic year: 2018
Degree: BACHELOR'S DEGREE IN INFORMATICS ENGINEERING (Syllabus 2010). (Teaching unit Optional)
ECTS credits: 6  Teaching languages: Catalan, Spanish

Teaching staff
Coordinator: - Angel Olivé Duran (angel@ac.upc.edu)

Prior skills

Requirements
- Prerequisite AC

Degree competences to which the subject contributes
Specific:
CEC1.1. To design a system based on microprocessor/microcontroller.
CEC1.2. To design/configure an integrated circuit using the adequate software tools.
CEC2.1. To analyse, evaluate, select and configure hardware platforms for the development and execution of computer applications and services.
CEC3.2. To develop specific processors and embedded systems; to develop and optimize the software of these systems.
CT6.2. To demonstrate knowledge, comprehension and capacity to evaluate the structure and architecture of computers, and the basic components that compound them.
CT7.1. To demonstrate knowledge about metrics of quality and be able to use them.

Generical:
G9. PROPER THINKING HABITS: capacity of critical, logical and mathematical reasoning. Capacity to solve problems in her study area. Abstraction capacity: capacity to create and use models that reflect real situations. Capacity to design and perform simple experiments and analyse and interpret its results. Analysis, synthesis and evaluation capacity.

Teaching methodology
In the theory classes expose the concepts of the course with student participation.
The exercise classes the students apply the theoretical concepts in solving exercises.
In laboratory classes students work in small groups and apply the concepts on a simple pipelined processor.

Learning objectives of the subject
1. Understanding concurrency techniques transparent to the programmer of machine language used by processors to reduce the execution time.
2. Understand some of the technological constraints in the implementation of a processor.
3. Knowledge of a hardware description language (VHDL) and application in the design of digital systems.
4. Training to assess the performance of a processor.
6. Basic understanding of the processor microarchitecture.

Study load

<table>
<thead>
<tr>
<th>Total learning time: 150h</th>
<th>Theory classes: 30h</th>
<th>20.00%</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Practical classes: 15h</td>
<td>10.00%</td>
</tr>
<tr>
<td></td>
<td>Laboratory classes: 15h</td>
<td>10.00%</td>
</tr>
<tr>
<td></td>
<td>Guided activities: 6h</td>
<td>4.00%</td>
</tr>
<tr>
<td></td>
<td>Self study: 84h</td>
<td>56.00%</td>
</tr>
</tbody>
</table>
## Content

### Von-Neumann architecture and performance.

**Degree competences to which the content contributes:**

**Description:**


### Techniques to increase the number of operations per unit time.

**Degree competences to which the content contributes:**

**Description:**

Pipelining and replication. Interpretation of instructions. Structural hazards.

### Linear pipeline processor.

**Degree competences to which the content contributes:**

**Description:**


### Techniques to reduce and tolerate the pipeline effective latency.

**Degree competences to which the content contributes:**

**Description:**

Static instruction scheduling. Data bypasses. Fixed branch prediction.

### Pipeline with multicycle operations.

**Degree competences to which the content contributes:**

**Description:**

## Planning of activities

<table>
<thead>
<tr>
<th>Topic</th>
<th>Hours</th>
<th>Description</th>
<th>Specific objectives</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Design tools and simulation</strong></td>
<td>15h</td>
<td>Learning tools for specification and simulation of logic circuits. Review of the operation and basic characteristics of the components of a single-cycle datapath.</td>
<td>3</td>
</tr>
<tr>
<td><strong>Von-Neumann machine and performance</strong></td>
<td>16h</td>
<td>Development of item 1 of the course</td>
<td>2, 4</td>
</tr>
<tr>
<td><strong>Techniques to increase the number of operations per unit time</strong></td>
<td>18h</td>
<td>Development of item 2 of the course</td>
<td>1, 4, 6</td>
</tr>
<tr>
<td><strong>Linear pipeline processor</strong></td>
<td>28h</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Partial Test

<table>
<thead>
<tr>
<th>Description</th>
<th>Specific objectives:</th>
<th>Hours: 10h</th>
</tr>
</thead>
</table>
| Development of item 3 of the course | 1, 4, 6 | Guided activities: 2h  
Self study: 8h |

| Specific objectives: | 1, 2, 4, 6 |

## Techniques to reduce and tolerate pipeline effective latency

<table>
<thead>
<tr>
<th>Description</th>
<th>Specific objectives:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Development of item 4 of the course</td>
<td>1, 4, 6</td>
</tr>
</tbody>
</table>

| Hours: 30h |
| Theory classes: 7h  
Practical classes: 4h  
Laboratory classes: 5h  
Guided activities: 0h  
Self study: 14h |

## Processor with multicycle operations

<table>
<thead>
<tr>
<th>Description</th>
<th>Specific objectives:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Development of item 5 of the course</td>
<td>1, 4, 6</td>
</tr>
</tbody>
</table>

| Hours: 19h |
| Theory classes: 5h  
Practical classes: 3h  
Laboratory classes: 0h  
Guided activities: 0h  
Self study: 11h |

## Consolidation

| Hours: 3h |
| Theory classes: 0h  
Practical classes: 0h  
Laboratory classes: 0h  
Guided activities: 3h  
Self study: 0h |
Final Exam

<table>
<thead>
<tr>
<th>Final Exam</th>
<th>Hours: 11h</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Guided activities: 3h</td>
</tr>
<tr>
<td></td>
<td>Self study: 8h</td>
</tr>
</tbody>
</table>

**Specific objectives:**
1, 2, 3, 4, 6

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**Qualification system**

There are three elements:

Final (F): final written exam covering all the objectives of the course. Partial (P): written test on the first three topics. Lab (L) from the reports made in each of the sessions and, where appropriate, a personal interview.

\[ NF = 0.2 \times L + \max[0.8 \times F, (0.65 \times F + 0.15 \times P)] \]

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**Bibliography**

**Basic:**


**Complementary:**