320098 - ELOD - Digital Electronics

Degree competences to which the subject contributes

Specific:
1. AUD_COMMON: The ability to analyse and design combinational, sequential, synchronous and asynchronous circuits and to use integrated-circuit microprocessors.
2. AUD_COMMON: Knowledge and application of the basic concepts underpinning the languages used to describe hardware.

General:
CG03. AUD: Knowledge of basic materials and technologies, enabling him to learn new methods and technologies and that will give the student versatility to adapt to new situations.
CG04. AUD: Ability to solve problems with initiative, decision making, creativity and communicate and transmit knowledge and skills, understanding the ethical and professional responsibility of the activity of Technical Telecommunications Engineering.
CG05. AUD: Knowledge to perform measurements, calculations, assessments, taxations, surveys, studies, reports, scheduling and similar work in their specific field of telecommunication.

Learning objectives of the subject

Teach students the theory behind the conception and design of digital systems. Familiarise students with CAD tools for digital system design and teach them how to implement them using programmable logic devices. Students will also be taught how to use the VHDL hardware description language, microprocessors and integrated circuits. This subject also aims to develop specific and transversal competencies associated with the coursework, as detailed below.
## Study load

<table>
<thead>
<tr>
<th>Total learning time: 150h</th>
<th>Hours large group: 15h</th>
<th>10.00%</th>
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</thead>
<tbody>
<tr>
<td>Hours medium group:</td>
<td>30h</td>
<td>20.00%</td>
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<tr>
<td>Hours small group:</td>
<td>15h</td>
<td>10.00%</td>
</tr>
<tr>
<td>Guided activities:</td>
<td>6h</td>
<td>4.00%</td>
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<tr>
<td>Self study:</td>
<td>84h</td>
<td>56.00%</td>
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</tbody>
</table>
### Content

<table>
<thead>
<tr>
<th>Topic 1: INTRODUCTION TO LOGIC CIRCUITS</th>
<th>Learning time: 17h</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description:</td>
<td>Theory classes: 2h</td>
</tr>
<tr>
<td>- Basic logic operations</td>
<td>Practical classes: 4h</td>
</tr>
<tr>
<td>- Analysis of logic circuits</td>
<td>Laboratory classes: 2h</td>
</tr>
<tr>
<td>- Logic gate synthesis</td>
<td>Self study: 9h</td>
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<tr>
<td>- Integrated circuit technology</td>
<td></td>
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<tr>
<td>- Standard integrated circuits</td>
<td></td>
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<tr>
<td>- Programmable logic devices</td>
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</tbody>
</table>

**Related activities:**
- Problem-based lectures
- Activity 1 and activity 2 are carried out. Activity 1 is an individual continuous assessment test to be completed outside class hours. The description and materials are available on the Atenea digital campus. Activity 2 is a directed practical laboratory exercise.

<table>
<thead>
<tr>
<th>Topic 2: PROGRAMMABLE LOGIC DEVICES AND VHDL</th>
<th>Learning time: 17h</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description:</td>
<td>Theory classes: 2h</td>
</tr>
<tr>
<td>- Low- and high-density programmable logic:</td>
<td>Practical classes: 4h</td>
</tr>
<tr>
<td>PLDs and FPGAs.</td>
<td>Laboratory classes: 2h</td>
</tr>
<tr>
<td>- Introduction to VHDL: entities, architectures, packets and libraries.</td>
<td>Self study: 9h</td>
</tr>
</tbody>
</table>

**Related activities:**
- Problem-based lectures
- Activity 2 is carried out. Activity 2 is a directed practical laboratory exercise.
### Topic 3: COMBINATIONAL LOGIC SYSTEMS

**Learning time:** 37h  
Theory classes: 4h  
Practical classes: 7h  
Laboratory classes: 4h  
Guided activities: 0h  
Self study: 22h

**Description:**  
- Combinational arithmetic circuits (adders, subtractors and comparators) and numeration systems  
- Arithmetic circuit design in VHDL  
- Multiplexers  
- Decoders/Demultiplexers  
- Encoders  
- Combinatorial block design in VHDL

**Related activities:**  
Problem-based lectures  
Activity 2 and activity 3 are carried out. Activity 2 is a directed practical laboratory exercise. Activity 3 is a problem-solving exercise.

### Topic 4: SEQUENTIAL LOGIC SYSTEMS

**Learning time:** 35h  
Theory classes: 3h  
Practical classes: 7h  
Laboratory classes: 5h  
Guided activities: 0h  
Self study: 20h

**Description:**  
- Flip-Flops (D flip-flop, T flip-flop and JK flip-flop)  
- Registers (shift registers, Enable entry registers)  
- Register design in VHDL  
- Counters (asynchronous and synchronous)  
- Counter design in VHDL

**Related activities:**  
Problem-based lectures  
Activity 1 is carried out. Activity 1 is an individual continuous assessment test to be completed outside class hours. The description and materials are available on the Atenea digital campus. Activity 2 is a directed practical laboratory exercise.
### Topic 5: SYNCHRONOUS SEQUENTIAL CIRCUITS

**Learning time:** 44h
- Theory classes: 4h
- Practical classes: 8h
- Laboratory classes: 2h
- Guided activities: 0h
- Self study: 30h

**Description:**
- Finite-state machines (FSMs)
- Moore model and Mealy model
- Synthesis of synchronous sequential circuits (state diagram and state transition table)
- Finite-state machine design in VHDL

**Related activities:**
Problem-based lectures
Activity 2 and activity 3 are carried out. Activity 2 is a directed practical laboratory exercise. Activity 3 is a problem-solving exercise.
### CONTINUOUS ASSESSMENT TEST (TOPIC 1, 3 AND 4)

**Description:**
Making individual autocorrect quizzes outside the classroom available in ATENEA with limited time and number of attempts. The questions and their order changes randomly, there are a database with different questions. In case of multiple-choice questions, the options also change randomly. Subsequently, the teacher reviews the qualifications and makes a general reflection in the classroom about common mistakes in order to clarify the main concepts of this activity.

**Support materials:**
Lectures note an exercise collection. Quizzes with different types of questions, multiple choice and short answer, available in ATENA.

**Descriptions of the assignments due and their relation to the assessment:**
The quizzes are available in the digital campus ATENEA. The questionnaire results represent 5% of the final mark.

**Specific objectives:**
After the activity, the student should be able to:
- Represent numbers in binary, octal and hexadecimal.
- Convert between decimal, binary, octal and hexadecimal number systems.
- Perform arithmetic operations in the binary system.
- Analyze and synthesize logic circuits.
- Know the basic devices for implementing sequential logic systems.
- Learn the most commonly used sequential blocks and applications.
- Analyze and synthesize digital circuits using sequential building blocks.

### LAB ASSIGNMENTS (TOPIC 1, 2, 3, AND 4)

**Hours:** 25h
- Laboratory classes: 15h
- Self study: 10h

**Description:**
The Lab sessions involve teams of two students. In these sessions, the students will carry out the design, simulation and implementation of combinational and sequential circuits using CAD tools for designing digital circuits. The students have to do a Pre-Lab report as autonomous learning before the lab session.

**Support materials:**
Tutorial and documentation about software and hardware platform used in the laboratory and the laboratory assignments. The laboratory assignments and supporting documentation is available in the digital campus ATENEA.

**Descriptions of the assignments due and their relation to the assessment:**
The Pre-Lab report and the Lab report can be required. The Pre-Lab and Lab reports are delivered by the digital campus ATENEA and represent 30% of the final mark.

**Specific objectives:**
At the end of each lab session, the student should be able to:
- Design, simulate and implement combinational and sequential logic circuits designs on state-of-the-art Programmable Logic Devices.
### PROBLEM SOLVING TEAM (TOPIC 3 AND 5)

**Description:**
Students outside the classroom prepare different exercises proposed in ATENEA, where they have to apply specific learning objectives with the related topics.

**Support materials:**
Exercise collection. The student may bring all the theoretical material that he thinks it is needed.

**Descriptions of the assignments due and their relation to the assessment:**
The exercise solutions are delivered through digital campus ATENEA. The exercise solutions represent 5% of the final mark.

**Specific objectives:**
At the end of these activities, the student should be able to:
- Analyze and synthesize digital circuits using combinational blocks.
- Analysis and synthesis of synchronous sequential digital circuits.
- Understand the operation of a microprocessor-based system.

### FIRST-SEMESTER EXAMINATION (TOPIC 1, 2, AND 3)

**Hours:** 9h
- Theory classes: 3h
- Self study: 6h

**Description:**
Single Test in classroom solving different problems related to learning objectives of the subject contents to the first-semester (2h 30min).

**Support materials:**
Exam.

**Descriptions of the assignments due and their relation to the assessment:**
Exam solution. The solution of the exam represents 25% of the final mark.

**Specific objectives:**
After the exam, the student should be able to:
- Represent and perform arithmetic on numbers in the binary system.
- Analyze and synthesize combinational logic circuits.

### SECOND-SEMESTER EXAMINATION (TOPIC 3, 4, AND 5)

**Hours:** 9h
- Theory classes: 3h
- Self study: 6h

**Description:**
Single Test in classroom solving different problems related to learning objectives of the subject contents to the second-semester (2h 30m).
Support materials:
Exam.

Descriptions of the assignments due and their relation to the assessment:
Exam solution. The solution of the exam represents 35% of the final mark.

Specific objectives:
After the exam, the student should be able to:
- Analyze and design combinational and sequential circuits, synchronous and asynchronous.
- Know and apply the different technologies of integrated circuits.

Qualification system
Oral and written exams 60% (25% First-semester examination, 35% Second-semester examination).
Laboratory sessions 30%.
Other Delivery Questionnaires and Solve exercises 10%.
For those students who meet the requirements and submit to the reevaluation examination, the grade of the reevaluation exam will replace the grades of all the on-site written evaluation acts (tests, midterm and final exams) and the grades obtained during the course for lab practices, works, projects and presentations will be kept.
If the final grade after reevaluation is lower than 5.0, it will replace the initial one only if it is higher. If the final grade after reevaluation is greater or equal to 5.0, the final grade of the subject will be pass 5.0.

Bibliography
Basic:

Complementary:

Others resources:
- Lecture notes available in the virtual campus ATENEA.