Last update: 05-07-2019

340375 - ESC2-I3O01 - Computer Structure II

Coordinating unit: 340 - EPSEVG - Vilanova i la Geltrú School of Engineering

Teaching unit: 701 - AC - Department of Computer Architecture

Academic year: 2019

Degree: BACHELOR'S DEGREE IN INFORMATICS ENGINEERING (Syllabus 2018). (Teaching unit Compulsory)
BACHELOR'S DEGREE IN INFORMATICS ENGINEERING (Syllabus 2010). (Teaching unit Compulsory)

ECTS credits: 6 Teaching languages: Catalan, Spanish

Teaching staff

Coordinator: Eva Marín Tordera

Degree competences to which the subject contributes

Specific:

1. CEFC1. Ability to design, develop, select and value applications and informatic systems affirming its reliability, security and quality corresponding to ethical principals and legislation and current rules.
2. CEFC13. Knowledge and application of necessary tools for storage, processing and access to informatic systems, including the ones based on webs.
3. CEFC4. Ability to work out technical conditions of an informatic installation observing standard and current rules.
4. CEFC7. Knowledge, design and efficient use of data types and structures the most appropriate to resolve problems.
5. CEFC9. Ability to know, understand and assess computer structure and architecture, as well as basic components forming them.

Transversal:

7. SUSTAINABILITY AND SOCIAL COMMITMENT - Level 2. Applying sustainability criteria and professional codes of conduct in the design and assessment of technological solutions.
6. THIRD LANGUAGE. Learning a third language, preferably English, to a degree of oral and written fluency that fits in with the future needs of the graduates of each course.

Learning objectives of the subject

Deeper knowledge of the structure of computers, as well as in the design and implementation of small micro-computer based systems. Specifically, it aims to understand and delve into the internal structures and the memory hierarchy (disk, main memory, caches, mechanisms for error detection and correction) in the concepts of concurrency, input / output and buses (survey, interruptions, DMA, types of I / S), and firmware programming of a microcomputer will also be addressed.

Last update: 05-07-2019

340375 - ESC2-I3O01 - Computer Structure II

Study load

Total learning time: 150h	Hours large group:	45h	30.00%
	Hours medium group:	0h	0.00%
	Hours small group:	15h	10.00%
	Guided activities:	0h	0.00%
	Self study:	90h	60.00%

Last update: 05-07-2019

340375 - ESC2-I3O01 - Computer Structure II

Content

1. Input/output

Learning time: 39h

Theory classes: 4h
Practical classes: 8h
Laboratory classes: 4h
Guided activities: 2h
Self study : 21h

Description:
1.1. Devices E/S: Polling
1.2. Synchronizing E/S for Interruptions
1.2.B Exceptions
1.3. Direct Memory Access (DMA)

Related activities:
Activity 1: Problems Input / Output
Activity 2: Lab 1 of synchronization by polling
Activity 2: Lab 2 of synchronization by interruptions
Activity 4: Partial test of knowledge

2. Cache Memory

Learning time: 30h

Theory classes: 4h
Practical classes: 7h
Laboratory classes: 2h
Guided activities: 2h
Self study : 15h

Description:
2.1. Introduction to Memory Hierarchy
2.2. Cache memory
2.3. Impact of the Organization of memory cache performance
2.4. Performance Measures
2.5 Design Considerations and cache controller

Related activities:
Activity 1: Cache memory exercises
Activity 2: Memory cache lab

340375 - ESC2-I3O01 - Computer Structure II

(ENG) 3. Memoria Virtual	Learning time: 20h Theory classes: 2h Practical classes: 4h Laboratory classes: 2h Guided activities: 2h Self study : 10h

Description:
3.1. Introduction
3.2. Address translation and pagination
3.3. Integrating virtual memory and cache

Related activities:
Activity 1: Virtual memory exercises

4. Microprogramming	Learning time: 29h Theory classes: 3h Practical classes: 6h Laboratory classes: 2h Self study : 18h

Description:

4.1. Revision Control Unit (INCO)
4.2. Types of Control Unit
4.3. Microprogrammed control unit

Related activities:
Activity 1: Microprogramming exercises
Activity 3: Work directed
Activity 4: Test of knowledge

Qualification system

Final Mark = (1st Partial knowledge test)*0,25 + (Exercises)*0,1 + (Lab)*0,2 + (Complementary work)*0,1 + (2nd partial knowledge test)*0,35 >=5
The second partial exam may be a partial exam with a weight of 35% or a final exam with a weight of 60% in order to recover the first partial (the student chooses what to do). In this second case the formula is:
Problems * 0.1 + Laboratory * 0.2 + complementary work * 0.1 + Final knowledge test * 0.6> = 5
The 1st and 2nd partial knoweledge tests are reevaluable (o final)

Last update: 05-07-2019

340375 - ESC2-I3O01 - Computer Structure II

Bibliography

Basic:

Patterson, David A. Computer organization and design : the hardware/software interface. 5a ed. Burlington [etc.]: Elsevier Morgan Kaufmann, cop. 2014. ISBN 9780124077263.