340378 - ARCO-I4001 - Computer Architecture

Coordinating unit: 340 - EPSEVG - Vilanova i la Geltrú School of Engineering
Teaching unit: 701 - AC - Department of Computer Architecture
Academic year: 2019
Degree: BACHELOR'S DEGREE IN INFORMATICS ENGINEERING (Syllabus 2018). (Teaching unit Compulsory)
BACHELOR'S DEGREE IN INFORMATICS ENGINEERING (Syllabus 2010). (Teaching unit Compulsory)
ECTS credits: 6 Teaching languages: Catalan, Spanish

Teaching staff
Coordinator: Eva Marín Tordera
Others: Eva Marín Tordera

Prior skills
It is recommendable to have studied ESC2.

Degree competences to which the subject contributes

Specific:
2. CEFC2. Ability to plan, conceive, develop, manage informatic projects, services and systems in all areas, leading their implementation and continuous improvement assessing their economic and social repercussions.
3. CEFC7. Knowledge, design and efficient use of data types and structures the most appropriate to resolve problems.
4. CEFC8. Ability to analyze, to design, to construct and to maintain applications in a well built, secure and efficient way choosing the most adequate paradigms and languages.
5. CEFC9. Ability to know, understand and assess computer structure and architecture, as well as basic components forming them.
6. CEFC14. Knowledge and application of fundamental principles and basic techniques of parallel, concurrent, distributed and real time programming.
7. CEFC17. Ability to design and evaluate computer interfaces that guarantee accessibility and usability of informatic systems, services and applications.

Transversal:
8. SUSTAINABILITY AND SOCIAL COMMITMENT - Level 3. Taking social, economic and environmental factors into account in the application of solutions. Undertaking projects that tie in with human development and sustainability.
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Teaching methodology

Theory classes are conducted using the resources available in the classroom (whiteboards, multimedia equipment) and are based on oral exposure by teachers of content on the subject under study (expository method). In some cases, there will be lectures based on the participation and involvement of students through short-term activities in the classroom, such as direct questioning, student presentations on specific topics or resolution of problems related to the theoretical exposed. Also the teacher will solve classroom exercises and propose collection exercises for students to prepare them independently. These exercises will be solved in class by the students individually or in groups.

Small group classes are:
- Laboratory classes: be performed on school computer classrooms. The student must take practice prepared (read and understand the statement of the practice from a script that was previously found in digital campus), and sometimes if indicated shall make a preliminary report. The practices will be individual.

Learning objectives of the subject

The main objectives of this course are:
- Programming in assembly language processor (RISC and CISC) "and link with high-level languages
- Introduction to Linear segmented processors and multiprocessors
- Architecture Graphic Cards

Study load

<table>
<thead>
<tr>
<th>Total learning time: 150h</th>
<th>Hours large group: 45h</th>
<th>30.00%</th>
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<tbody>
<tr>
<td></td>
<td>Hours medium group: 0h</td>
<td>0.00%</td>
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<tr>
<td></td>
<td>Hours small group: 15h</td>
<td>10.00%</td>
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<tr>
<td></td>
<td>Guided activities: 0h</td>
<td>0.00%</td>
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<tr>
<td></td>
<td>Self study: 90h</td>
<td>60.00%</td>
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<table>
<thead>
<tr>
<th>Content</th>
<th>Learning time: 8h</th>
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| **1. Introduction** | Theory classes: 1h  
Practical classes: 1h  
Self study: 6h |
| **Description:** | Performance, CPI, Speed-up, Amdhal's Law, Power, Consumption |
| **Related activities:** | Activity 1: Introduction problems |

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<tr>
<th><strong>2. Introduction to MIPS. Assembly language</strong></th>
<th>Learning time: 21h</th>
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| Theory classes: 2h  
Practical classes: 5h  
Laboratory classes: 2h  
Self study: 12h |
| **Description:** | Introduction to MIPS assembler. Type of data. Memory addressing. Translation from assembler to C and from C to assembler |
| **Related activities:** | Activity 1: Assembler problems  
Activity 2: Practice in assembler MIPS. Practice 0: Introduction to QtSpim |

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<tr>
<th><strong>3. Assembler MIPS-Subroutines</strong></th>
<th>Learning time: 31h</th>
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| Theory classes: 3h  
Practical classes: 6h  
Laboratory classes: 4h  
Self study: 18h |
| **Description:** | Subroutines in MIPS. Instructions, steps in a subroutine, nested subroutines, the stack. |
| **Related activities:** | Activity 1: Subroutine problems  
Activity 2: Practice assembler MIPS. Practice 1: Subroutines in MIPS |
## 4. Introduction to pipelining, parallelism and multiprocessors

### Description:
- 4.1 Pipelining
- 4.2 Parallelism
- 4.3 Scalar and vector processors
- 4.4 Graphic cards architecture

### Related activities:
- Activity 1: Pipelining problems
- Activity 2. Practice with the pipeline MIPS processor. Practice 2. The MIPS pipelining processor with MIPSIt 2000
- Activity 3: Directed work
- Activity 4: Knowledge test

### Learning time: 22h
- Theory classes: 2h
- Practical classes: 4h
- Laboratory classes: 2h
- Guided activities: 2h
- Self study: 12h

## 5. Memory

### Description:
Review of memory cache. Policies on failure, writing policies. Main Memory (from the basic cell to the DDR), refresh, DIMM DDR.

### Related activities:
- Activity 1: Memory problems
- Activity 2: Practice assembler MIPS. Practice 3: Software Memory Cache

### Learning time: 20h
- Theory classes: 2h
- Practical classes: 4h
- Laboratory classes: 2h
- Self study: 12h
6. Input/Output

Learning time: 20h
- Theory classes: 2h
- Practical classes: 4h
- Laboratory classes: 2h
- Guided activities: 0h
- Self study: 12h

Description:
Review of Input/Output studied in ESC2 extended to RAIDs, flash memories, buses, performance of the I/O system.

Related activities:
Activity 1: I/O problems

Qualification system
Partial knowledge 1er test * 0.25 + problems * 0.1 + 0.25 * Laboratory + complementary work * 0.1 + partial knowledge 2nd Test * 0.3 > = 5
The second partial exam can be a 2nd partial exam with a weight of 30% or a final exam with a weight of 55% in order to recover the first partial (the student chooses what to do). In this second case the formula is:
Problems * 0.1 + Laboratory * 0.25 + complementary work * 0.1 + Final knowledge test * 0.55 > = 5
The 1st and 2nd partial knowledge tests are reevaluable (o final)

Regulations for carrying out activities
Activities 1, 2 and 4 are in person.
Activity 3 is non-attendance, although there may be a short presentation in class.
In the activities that take place in the qualifying group will be the same for all group members

Bibliography
Basic:

Others resources:
Computer material
Software proporcionat a l’assignatura
Software provided in the course: QtSpim i MipsIT