Course guide
820241 - DMD - Digital Microelectronic Design

Unit in charge: Barcelona East School of Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.
Degree: BACHELOR’S DEGREE IN INDUSTRIAL ELECTRONICS AND AUTOMATIC CONTROL ENGINEERING (Syllabus 2009). (Optional subject).
Academic year: 2022  ECTS Credits: 6.0  Languages: English

LECTURER
Coordinating lecturer: Cosp Vilella, Jordi
Others: Segon quadrimestre: JORDI COSP VILELLA - M11

PRIOR SKILLS
To have completed the course on Digital Electronics and Electronic Technology

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
1. Design analogue, digital and power systems.

Transversal:
2. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 3. Communicating clearly and efficiently in oral and written presentations. Adapting to audiences and communication aims by using suitable strategies and means.
3. EFFECTIVE USE OF INFORMATION RESOURCES - Level 3. Planning and using the information necessary for an academic assignment (a final thesis, for example) based on a critical appraisal of the information resources used.

TEACHING METHODOLOGY
The teacher will show digital integrated circuit (chip) analysis and design procedures and how to configure commercial programmable logic devices (FPGAs and CPLDs) and some exercices to be solved by students will be proposed during the course.
In parallel, at the lab, the student will learn how to use electronic design computer tools to perform its own designs and to settle the learned concepts during lecture sessions.
A small design project on a digital electronic circuit will be also developed and experimentally verified using high level design tools (VHDL).

LEARNING OBJECTIVES OF THE SUBJECT
To learn how to analyze and design electronic integrated digital circuits on applications specific circuits (ASIC) or standard programmable logic devices (PLD) using high level hardware description languages.
To learn how to analyze and design the basic elements that constitute a digital electronic circuit.
To learn how to use the tools for Electronic Design Automation (EDA) that are available on the market.
STUDY LOAD

<table>
<thead>
<tr>
<th>Type</th>
<th>Hours</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hours large group</td>
<td>45,0</td>
<td>30.00</td>
</tr>
<tr>
<td>Self study</td>
<td>90,0</td>
<td>60.00</td>
</tr>
<tr>
<td>Hours small group</td>
<td>15,0</td>
<td>10.00</td>
</tr>
</tbody>
</table>

Total learning time: 150 h

CONTENTS

Introduction to Microelectronics

Description:
Introduction and basic concepts of microelectronic technology and design

Specific objectives:
To be introduced to microelectronic basics.

Related activities:
None

Related competencies:
CEEIA-24. Design analogue, digital and power systems.
06 URI N3. EFFECTIVE USE OF INFORMATION RESOURCES - Level 3. Planning and using the information necessary for an academic assignment (a final thesis, for example) based on a critical appraisal of the information resources used.
04 COE N3. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 3. Communicating clearly and efficiently in oral and written presentations. Adapting to audiences and communication aims by using suitable strategies and means.

Full-or-part-time: 5h
Theory classes: 2h
Self study : 3h

High Level Hardware Description of Integrated Circuits (VHDL)

Description:
The VHDL language and its application to integrated digital circuit design
Concurrent statements
Sequential statements
Testbench generation
Restriction files generation
Digital design advanced concepts

Specific objectives:
To learn how to design digital systems using high level hardware descriptions.

Related activities:
Development of a digital design using the high level hardware description language VHDL and practical verification of its functionality on a programmable device (FPGA)

Full-or-part-time: 54h 30m
Theory classes: 19h
Laboratory classes: 7h
Self study : 26h 30m
**Review of MOS Transistor Fundamentals**

**Description:**
- MOS transistor models and basic concepts
- MOS transistor characteristic curves
- Modes of operation
- NMOS transistor vs PMOS transistor
- The current source

**Specific objectives:**
To know the basics of MOS transitors and to be able to use correctly these models in circuit design and analysis.

**Related activities:**
To obtain the current-voltage curve of type N and P MOS transistors by simulations and extract their most important parameters.

**Related competencies:**
- CEEIA-24. Design analogue, digital and power systems.
- 06 URI N3. EFFECTIVE USE OF INFORMATION RESOURCES - Level 3. Planning and using the information necessary for an academic assignment (a final thesis, for example) based on a critical appraisal of the information resources used.
- 04 COE N3. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 3. Communicating clearly and efficiently in oral and written presentations. Adapting to audiences and communication aims by using suitable strategies and means.

**Full-or-part-time:** 18h
- Theory classes: 4h
- Laboratory classes: 2h
- Self study: 12h

**The microelectronic Process**

**Description:**
- Introduction
- Description of the VLSI microelectronic process
- The layout

**Specific objectives:**
To know what the manufacturing process of CMOS integrated circuits is and understand its implications on the behaviour and performance of this kind of circuits.

**Related activities:**
To draw an elementary microelectronic circuit layout.

**Related competencies:**
- CEEIA-24. Design analogue, digital and power systems.
- 06 URI N3. EFFECTIVE USE OF INFORMATION RESOURCES - Level 3. Planning and using the information necessary for an academic assignment (a final thesis, for example) based on a critical appraisal of the information resources used.
- 04 COE N3. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 3. Communicating clearly and efficiently in oral and written presentations. Adapting to audiences and communication aims by using suitable strategies and means.

**Full-or-part-time:** 10h
- Theory classes: 4h
- Self study: 6h
**The MOS Inverter**

**Description:**
CMOS inverter structure  
DC inverter behaviour  
Dynamic inverter behaviour

**Specific objectives:**
To understand the behaviour of a CMOS inverter, to be able to analyze its static and dynamic behaviour and to be able to design it according to a certain specs.

**Related activities:**
Design and verify the behaviour through simulations of a CMOS inverter.

**Related competencies:**
CEEIA-24. Design analogue, digital and power systems.
06 URI N3. EFFECTIVE USE OF INFORMATION RESOURCES - Level 3. Planning and using the information necessary for an academic assignment (a final thesis, for example) based on a critical appraisal of the information resources used.
04 COE N3. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 3. Communicating clearly and efficiently in oral and written presentations. Adapting to audiences and communication aims by using suitable strategies and means.

**Full-or-part-time:** 21h 30m
Theory classes: 6h  
Laboratory classes: 2h  
Self study : 13h 30m

**Static Logic Gates**

**Description:**
Description of NAND and NOR static gates  
DC behaviour of the NAND and NOR gates  
Dynamic behaviour of NAND and NOR gates  
AND-OR-INVERTER logic  
CMOS transmission gate

**Specific objectives:**
To understand the behaviour of a CMOS logical gate, to be able to analyze its static and dynamic behaviour and to be able to design it according to a certain specs.

**Related activities:**
Design and verify the behaviour through simulations of a CMOS logic gate.

**Related competencies:**
CEEIA-24. Design analogue, digital and power systems.
06 URI N3. EFFECTIVE USE OF INFORMATION RESOURCES - Level 3. Planning and using the information necessary for an academic assignment (a final thesis, for example) based on a critical appraisal of the information resources used.
04 COE N3. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 3. Communicating clearly and efficiently in oral and written presentations. Adapting to audiences and communication aims by using suitable strategies and means.

**Full-or-part-time:** 23h
Theory classes: 6h  
Laboratory classes: 2h  
Self study : 15h
Sequential Circuits

Description:
The RS latch
The level triggered latch
The edge triggered flip-flop

Specific objectives:
To understand the behaviour of a CMOS flip-flop, to be able to analyze its static and dynamic behaviour and to be able to design it according to a certain specs.

Related activities:
Design and verify the behaviour through simulations of a CMOS flip-flop.

Related competencies:
CEEIA-24. Design analogue, digital and power systems.
06 URI N3. EFFECTIVE USE OF INFORMATION RESOURCES - Level 3. Planning and using the information necessary for an academic assignment (a final thesis, for example) based on a critical appraisal of the information resources used.
04 COE N3. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 3. Communicating clearly and efficiently in oral and written presentations. Adapting to audiences and communication aims by using suitable strategies and means.

Full-or-part-time: 18h
Theory classes: 4h
Laboratory classes: 2h
Self study : 12h

GRADING SYSTEM

Midcourse exam: 10%; Final written test 25% Laboratory exercises: 25% Design project: 40%

EXAMINATION RULES.

It is required to have completed the laboratory exercise and bring the ID card or other identification on the day of testing.

BIBLIOGRAPHY

Basic:

Complementary: