230642 - AACT - Advanced Analog Circuit Techniques

Coordinating unit: 230 - ETSETB - Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering
Academic year: 2019
Degree: MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2013). (Teaching unit Compulsory)
MASTER'S DEGREE IN ADVANCED TELECOMMUNICATION TECHNOLOGIES (Syllabus 2019).
(Teaching unit Optional)
MASTER'S DEGREE IN TELECOMMUNICATIONS ENGINEERING (Syllabus 2013). (Teaching unit Optional)
MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2009). (Teaching unit Optional)
ECTS credits: 5  Teaching languages: English

Teaching staff
Coordinator: XAVIER ARAGONES CERVERA
Others: XAVIER ARAGONES CERVERA

Prior skills
The course assumes basic concepts of amplification, analog circuit analysis and transistor modeling, as well as circuit simulation environments such as Cadence or Spice, corresponding to the "Electronics for Communication Systems" bridge course or similar:
- MOSFET basic behavior: states, equations, curves
- BJT basic behavior: states, equations, curves
- Analog circuit analysis: large signal and small-signal
- Two-port modeling of amplifiers
- Basic 1-transistor amplifier stages
- Circuit simulation at transistor level (.DC, .TRAN, .AC analysis)
- Basic concepts on active-RC filters.
- Basic concepts on DAC and ADC conversion.

Requirements
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Degree competences to which the subject contributes
Specific:
1. Ability to conceive and design electronic circuits for signal amplification, for low and high (radio) frequencies, depending on the type of application and targeting specific consumption, noise, linearity, stability, impedance and bandwidth figures.
Learning objectives of the subject:

The aim of this course is to provide the student with knowledge of the main types of circuits involved in analog signal acquisition and processing (amplification, filtering and conversion from/to digital domain), with special focus on understanding the causes of main non-idealities that limit the dynamic range, resolution, precision, or the frequency of operation, and how different circuit solutions can cope with these limitations. After this course, the student will be in position to easily follow specialized courses focused on specific applications (e.g., high-frequency communications, signal conditioning) or specific technologies (e.g., microelectronics). The course assumes as previous knowledge: basic concepts of amplification, transistor modeling, analysis of analog circuits described at transistor level or two-port level, as well as circuit simulation environments such as Cadence or Spice, corresponding to the "Electronics for Communication Systems" leverage course or similar. Beyond these basic concepts, a first part of the course is devoted to describe and understand the limitations of basic amplification circuits -transistor-level- and introduce advanced circuit solutions and techniques. A second part of the course is devoted to analyze different solutions for filtering, both continuous-time and using the switched-capacitor approach, and understand the main characteristics of the different approaches. The last part of the course is devoted to analog-digital conversion, architectures for high resolution or high speed, evaluation of their figures of merit, with special focus on understanding the effects the limit the effective resolution and conversion speed.

Transversal:

4. EFFECTIVE USE OF INFORMATION RESOURCES: Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.
5. FOREIGN LANGUAGE: Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

Teaching methodology

- Lectures
- Individual work (distance)
- Design exercises (analysis and simulation)
- Extended answer test (Final Exam)

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Study load

<table>
<thead>
<tr>
<th>Total learning time: 125h</th>
<th>Hours large group: 39h</th>
<th>31.20%</th>
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<tbody>
<tr>
<td>Hours medium group: 0h</td>
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<td>0.00%</td>
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<tr>
<td>Hours small group: 0h</td>
<td></td>
<td>0.00%</td>
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<tr>
<td>Guided activities: 0h</td>
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<td>0.00%</td>
</tr>
<tr>
<td>Self study: 86h</td>
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<td>68.80%</td>
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</table>
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### Content

<table>
<thead>
<tr>
<th>1. Amplification</th>
<th>Learning time: 49h</th>
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<tbody>
<tr>
<td></td>
<td>Theory classes: 15h</td>
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<tr>
<td></td>
<td>Guided activities: 14h</td>
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<tr>
<td></td>
<td>Self study: 20h</td>
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**Description:**
- Review of Basic Single-Transistor Amplifier Stages, MOS and BJT. Biasing. Analysis of the performance (frequency response, linearity, power consumption) in function of the design decisions.
- Output stages. Solutions for matching to low impedances.
- Current mirrors and references.
- Analysis of the trade-off between bandwidth, gain and power consumption. Solutions to amplify at high frequencies (RF). Impact on linearity, variability.
- Open-loop amplification vs feedback-based. Compromise gain- bandwidth.
- High-gain Amplifier Stages: Cascode, active cascode, folded cascode.

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<tr>
<th>2. Continuous time and Switched capacitor filtering</th>
<th>Learning time: 43h</th>
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<tr>
<td></td>
<td>Theory classes: 12h</td>
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<tr>
<td></td>
<td>Guided activities: 11h</td>
</tr>
<tr>
<td></td>
<td>Self study: 20h</td>
</tr>
</tbody>
</table>

**Description:**
- Integrator-based continuous-time filters (active - RC)
- Variability: trimming, MOSFET - C
- Gm-C filters. Gm-cells.
- Switched capacitor circuits:
  - Principles
  - Switched capacitor integrators
- General topologies.
  - Bilinear and Biquad stages with continuous-time and discrete-time implementations.
  - Implementation of higher-order filters
3. Analog - Digital Conversion

Description:
- Digital / Analog converters:
  - Characterization, static linearity (DNL, INL), dynamic characteristics.
  - Parallel architectures. Binary and unary scaling. Segmentation.
  - Serial architectures.
- Analog / Digital converters:
  - Sample & hold circuits, limitations. Aliasing.
  - Characterization, static linearity (DNL, INL), dynamic characteristics.
  - Serial architectures. Successive approximations.
  - Parallel architectures. Comparators.
  - Pipeline. Time interleaving.

Learning time: 38h
- Theory classes: 12h
- Guided activities: 11h
- Self study: 15h

Qualification system

Final examination: 45%
Partial examination: 20%
Exercises: 35%

Bibliography

Basic:

Complementary:

Others resources:
Course slides, exercises, and tutorials available through the Atenea virtual campus.