230646 - MND - Micro and Nano Electronic Design

Coordinating unit: 230 - ETSETB - Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering
Academic year: 2019
Degree: MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2013). (Teaching unit Compulsory)
MASTER'S DEGREE IN ADVANCED TELECOMMUNICATION TECHNOLOGIES (Syllabus 2019).
(Teaching unit Optional)
MASTER'S DEGREE IN INFORMATION AND COMMUNICATION TECHNOLOGIES (Syllabus 2009).
(Teaching unit Optional)
MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2009). (Teaching unit Optional)
ECTS credits: 5
Teaching languages: English

Teaching staff
Coordinator: JORDI MADRENAS BOADAS
Others: FRANCESC MOLL ECHETO, JORDI COSP VILELLA
Madrenas Boadas, Jordi

Degree competences to which the subject contributes

Specific:
1. Ability to design CMOS digital and analog integrated circuits of medium complexity.
2. Ability to apply low-power techniques to integrated circuits (ICs).
3. Ability to design for testability and test schemes for ICs.

Transversal:
4. EFFECTIVE USE OF INFORMATION RESOURCES: Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.
5. FOREIGN LANGUAGE: Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

Teaching methodology
- Lectures
- Laboratory classes
- Laboratory practical work
- Group work (distance)
- Oral presentations
- Short answer test (Control)
- Extended answer test (Final Exam)

Learning objectives of the subject

Learning objectives of the subject:
The aim of this course is to train students in methods of integrated circuit design. First, state-of-the-art and trends in VLSI and their design implications are introduced. Then, basic analog and digital circuits are presented. In a second phase, low-power techniques and design for testability are developed. Lab projects are proposed to introduce the
practical aspects of VLSI design and the CAE tools.

Learning results of the subject:

- Ability to understand the evolution of integrated technologies.
- Ability to identify cases and applications suitable for an integrated solution.
- Ability to analyze the characteristics of a mixed-signal integrated circuit.
- Ability to design analog and digital medium-complexity CMOS integrated circuits.

<table>
<thead>
<tr>
<th>Study load</th>
<th>Hours large group:</th>
<th>Hours medium group:</th>
<th>Hours small group:</th>
<th>Guided activities:</th>
<th>Self study:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total learning time:</td>
<td>125h</td>
<td>26h</td>
<td>0h</td>
<td>13h</td>
<td>86h</td>
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<td>20.80%</td>
<td>0.00%</td>
<td>10.40%</td>
<td>68.80%</td>
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<tr>
<td>Content</td>
<td>Learning time:</td>
<td>Theory classes:</td>
<td>Laboratory classes:</td>
<td>Self study:</td>
<td></td>
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<tr>
<td>1. Introduction</td>
<td>8h</td>
<td>3h</td>
<td>5h</td>
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<tr>
<td>2. Basic digital blocks and their characterization</td>
<td>20h</td>
<td>7h</td>
<td>2h</td>
<td>11h</td>
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<tr>
<td>3. Basic analog blocks and their characterization</td>
<td>20h</td>
<td>7h</td>
<td>2h</td>
<td>11h</td>
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</tr>
</tbody>
</table>
### 4. Practical aspects of VLSI design

**Learning time:** 16h  
- Theory classes: 5h  
- Laboratory classes: 2h  
- Self study: 9h

**Description:**  
- Buffering.  
- Power and clock distribution.  
- Input/output pads. Packaging.  
- Low-power circuit- and architecture-level techniques.

### 5. Basic concepts of testing

**Learning time:** 12h  
- Theory classes: 4h  
- Laboratory classes: 2h  
- Self study: 6h

**Description:**  
- Design for testability. Test coverage. ATPG.  
- Design for manufacturability.

### 6. Laboratory of VLSI design

**Learning time:** 49h  
- Laboratory classes: 5h  
- Self study: 44h

**Description:**  
- Design of a transconductor.  
- Design of a simple digital processor.  
- Design project: digitally-assisted analog front-end.
## Planning of activities

### LABORATORY

**Description:**
- Introduction to CAE tools for VLSI. Design rules, layout, electric and logic simulation, synthesis, placement & routing, backannotation.
- Design of a transconductor.
- Design of a simple digital processor.
- Design project. Front-end and back-end.

### ORAL PRESENTATION

**Description:**
Presentation of a work group.

### SHORT ANSWER TEST (CONTROL)

**Description:**
Mid term control.

### EXTENDED ANSWER TEST (FINAL EXAMINATION)

**Description:**
Final examination.

## Qualification system

Final examination: 35%
Midterm examination: 35%
Laboratory assessments: 30%

## Bibliography

### Basic:


### Complementary:
