Learning objectives of the subject:

The aim of this course is to train students in methods of integrated circuit design. First, state-of-the-art and trends in VLSI and their design implications are introduced. Then, basic analog and digital circuits are presented. In a second phase, low-power techniques and design for testability are developed. Lab projects are proposed to introduce the practical aspects of VLSI design and the CAE tools.
Learning results of the subject:

- Ability to understand the evolution of integrated technologies.
- Ability to identify cases and applications suitable for an integrated solution.
- Ability to analyze the characteristics of a mixed-signal integrated circuit.
- Ability to design analog and digital medium-complexity CMOS integrated circuits.

### Study load

<table>
<thead>
<tr>
<th>Total learning time: 125h</th>
<th>Hours large group: 26h 20.80%</th>
<th>Hours medium group: 0h 0.00%</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Hours small group: 13h 10.40%</td>
<td>Guided activities: 0h 0.00%</td>
</tr>
<tr>
<td></td>
<td>Self study: 86h 68.80%</td>
<td></td>
</tr>
</tbody>
</table>

Last update: 06-05-2019
## Content

<table>
<thead>
<tr>
<th>Section</th>
<th>Learning time</th>
<th>Theory classes</th>
<th>Laboratory classes</th>
<th>Self study</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1. Introduction</strong></td>
<td><strong>8h</strong></td>
<td>3h</td>
<td></td>
<td>5h</td>
</tr>
<tr>
<td><strong>Description:</strong></td>
<td></td>
<td>Structure of static gates.</td>
<td>Manufacturing process. Masks. Layout.</td>
<td>MOSFET models.</td>
</tr>
<tr>
<td><strong>2. Basic digital blocks and their characterization</strong></td>
<td><strong>20h</strong></td>
<td>7h</td>
<td>2h</td>
<td>11h</td>
</tr>
<tr>
<td><strong>3. Basic analog blocks and their characterization</strong></td>
<td><strong>20h</strong></td>
<td>7h</td>
<td>2h</td>
<td>11h</td>
</tr>
</tbody>
</table>
# 4. Practical aspects of VLSI design

**Learning time:** 16h  
- Theory classes: 5h  
- Laboratory classes: 2h  
- Self-study: 9h

**Description:**  
- Buffering.  
- Power and clock distribution.  
- Input/output pads. Packaging.  
- Low-power circuit- and architecture-level techniques.

# 5. Basic concepts of testing

**Learning time:** 12h  
- Theory classes: 4h  
- Laboratory classes: 2h  
- Self-study: 6h

**Description:**  
- Design for testability. Test coverage. ATPG.  
- Design for manufacturability.

# 6. Laboratory of VLSI design

**Learning time:** 49h  
- Laboratory classes: 5h  
- Self-study: 44h

**Description:**  
- Post-layout simulation.  
- Design of a transconductor.  
- Design of a simple digital processor.  
- Design project: digitally-assisted analog front-end.
### Planning of activities

| LABORATORY
| Description: |
| - Introduction to CAE tools for VLSI. Design rules, layout, electric and logic simulation, synthesis, placement & routing, backannotation. |
| - Design of a transconductor. |
| - Design of a simple digital processor. |
| - Design project. Front-end and back-end. |

| ORAL PRESENTATION
| Description: |
| Presentation of a work group. |

| SHORT ANSWER TEST (CONTROL)
| Description: |
| Mid term control. |

| EXTENDED ANSWER TEST (FINAL EXAMINATION)
| Description: |
| Final examination. |

### Qualification system

- Final examination: 35%
- Midterm examination: 35%
- Laboratory assessments: 30%

### Bibliography

**Basic:**


**Complementary:**
