Course guides
230646 - MND - Micro and Nano Electronic Design

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2013). (Compulsory subject).
MASTER'S DEGREE IN TELECOMMUNICATIONS ENGINEERING (Syllabus 2013). (Optional subject).
MASTER'S DEGREE IN ADVANCED TELECOMMUNICATION TECHNOLOGIES (Syllabus 2019). (Optional subject).

Academic year: 2020 ECTS Credits: 5.0 Languages: English

LECTURER
Coordinating lecturer: JORDI MADRENAS BOADAS
Others: FRANCESC MOLL ECHETO, JORDI COSP VILELLA

Madrenas Boadas, Jordi

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
1. Ability to design CMOS digital and analog integrated circuits of medium complexity.
2. Ability to apply low-power techniques to integrated circuits (ICs).
3. Ability to design for testability and test schemes for ICs.

Transversal:
4. EFFECTIVE USE OF INFORMATION RESOURCES: Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.

5. FOREIGN LANGUAGE: Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

TEACHING METHODOLOGY

- Lectures
- Laboratory classes
- Laboratory practical work
- Group work (distance)
- Oral presentations
- Short answer test (Control)
- Extended answer test (Final Exam)
LEARNING OBJECTIVES OF THE SUBJECT

Learning objectives of the subject:

The aim of this course is to train students in methods of integrated circuit design. First, state-of-the-art and trends in VLSI and their design implications are introduced. Then, basic analog and digital circuits are presented. In a second phase, low-power techniques and design for testability are developed. Lab projects are proposed to introduce the practical aspects of VLSI design and the CAE tools.

Learning results of the subject:

- Ability to understand the evolution of integrated technologies.
- Ability to identify cases and applications suitable for an integrated solution.
- Ability to analyze the characteristics of a mixed-signal integrated circuit.
- Ability to design analog and digital medium-complexity CMOS integrated circuits.

STUDY LOAD

<table>
<thead>
<tr>
<th>Type</th>
<th>Hours</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hours large group</td>
<td>26,0</td>
<td>20.80</td>
</tr>
<tr>
<td>Self study</td>
<td>86,0</td>
<td>68.80</td>
</tr>
<tr>
<td>Hours small group</td>
<td>13,0</td>
<td>10.40</td>
</tr>
</tbody>
</table>

Total learning time: 125 h

CONTENTS

1. Introduction

Description:
- Structure of static gates.
- MOSFET models.
- State-of-the-art in VLSI. Full-custom and standard-cell design.

Full-or-part-time: 8h
Theory classes: 3h
Self study : 5h

2. Basic digital blocks and their characterization

Description:
- Parasitic elements. Delay definitions. Logical effort.
- Power dissipation.

Full-or-part-time: 20h
Theory classes: 7h
Laboratory classes: 2h
Self study : 11h
### 3. Basic analog blocks and their characterization

**Description:**
- Current sources and mirrors.
- Basic amplifier stages.
- Voltage and current references.
- Small-signal model. Parasitics and frequency response.

**Full-or-part-time:** 20h
- Theory classes: 7h
- Laboratory classes: 2h
- Self study: 11h

### 4. Practical aspects of VLSI design

**Description:**
- Buffering.
- Power and clock distribution.
- Input/output pads. Packaging.
- Low-power circuit- and architecture-level techniques.

**Full-or-part-time:** 16h
- Theory classes: 5h
- Laboratory classes: 2h
- Self study: 9h

### 5. Basic concepts of testing

**Description:**
- Design for testability. Test coverage. ATPG.
- Design for manufacturability.

**Full-or-part-time:** 12h
- Theory classes: 4h
- Laboratory classes: 2h
- Self study: 6h

### 6. Laboratory of VLSI design

**Description:**
- Design of a transconductor.
- Design of a simple digital processor.
- Design project: digitally-assisted analog front-end.

**Full-or-part-time:** 49h
- Laboratory classes: 5h
- Self study: 44h
ACTIVITIES

LABORATORY

Description:
- Introduction to CAE tools for VLSI. Design rules, layout, electric and logic simulation, synthesis, placement & routing, backannotation.
- Design of a transconductor.
- Design of a simple digital processor.
- Design project. Front-end and back-end.

ORAL PRESENTATION

Description:
Presentation of a work group.

SHORT ANSWER TEST (CONTROL)

Description:
Mid term control.

EXTENDED ANSWER TEST (FINAL EXAMINATION)

Description:
Final examination.

GRADING SYSTEM

Final examination: 35%
Midterm examination: 35%
Laboratory assessments: 30%

BIBLIOGRAPHY

Basic:

Complementary: