Last update: 24-03-2017

230652 - ESDC - Electronic System Design for Communications

Coordinating unit: 230 - ETSETB - Barcelona School of Telecommunications Engineering

Teaching unit: 710 - EEL - Department of Electronic Engineering

Academic year: 2017

Degree: MASTER'S DEGREE IN TELECOMMUNICATIONS ENGINEERING (Syllabus 2013). (Teaching unit Compulsory)

ECTS credits: 5 Teaching languages: English

Teaching staff

Coordinator: Rubio Sola, Jose Antonio
Moll Echeto, Francesc De Borja

Others: Rubio Sola, Jose Antonio
Moll Echeto, Francesc De Borja

Opening hours

Timetable: see consultation schedule for each professor in the web of the faculty

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Prior skills

Previous knowledge needed to follow all the explanations:
CONCEPTS OF PHYSICS:
- Plate parallel capacitance. Voltage-Charge relation. Dielectrics.
- Magnetic flux. Self-Inductance. Mutual Inductance.
- PN Junctions: forward and reverse biasing.
BASIC CIRCUIT ANALYSIS:
- RC circuits. Time constant. Energy stored in a capacitor.
- LR circuits. Time constant. Energy stored in a inductance.
- Concept of resonance frequency in RLC circuits.
MOS TRANSISTOR
- Identification of terminals, sing of currents and voltages in NMOS and PMOS devices.
- Large Signal (DC), long channel equations (ID vs VGS, VDS) curves and regions. Transconductance and gate dimensions. Channel-Length modulation. Overdrive voltage
- Unified model for PMOS and NMOS.
- Threshold voltage effects: Body Effect. Threshold voltage as a function of bulksource voltage: linear simplification equation. Drain induced barrier lowering.
- Short channel equations: Mobility degradation and Velocity saturation.
- Parasitic capacitances: Gate capacitance and Diffusion Capacitance
DIGITAL CIRCUITS
- CMOS Logic gates. Extraction of the truth table and logic expression form a gate transistor schematic.
- Pass Transistor DC characteristics. N, P and CMOS transmission gates.
- Inverter: Static transfer function. Noise Margin definition.
DIGITAL DESIGN
- Digital codes: Signed and unsigned binary codes. Basic binary arithmetic operations: addition and multiplication. Error Detection Codes: parity codes.
- Combinational circuits. Canonical implementation of logic functions. De Morgan?s Laws.
- State Machines: state diagram. Canonical structure of sequential systems.
- Basic combinational and seqüential blocks. Truth table. Logic level schematic. Symbol. (basic logic gates, multiplexer, decoder, half adder, full adder, flip-flop, latch, register, counter).
- Digital waveform as a function of time interpretation.
- VHDL Hardware Description Language.
- Basic understanding of C programming
- Basic microprocessor experience
DATA COMMUNICATIONS BASICS (*)
- Basics of data flow and digital communication channels
- Types of network connections
- Network topologies
- Network types (LAN, WLAN)
- Switched WAN
- Packet switching Networks
- Internet basics
- Communication protocols
- Protocols layering
- TCP/IP protocol
- Layers communication in networks with switching and routers
- Message encapsulation and decapsulation
- Addressing in TCP/IP protocol suite

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- Multiplexing and demultiplexing
- OSI model
- Time Division and Frequency Division Multiplexing
(*) For this part we suggest ?Data Communications and Networking? of B.A. Forouzan

Degree competences to which the subject contributes

Specific:

1. Ability to design and manufacture integrated circuits

2. Knowledge of hardware description languages for high-complex circuits.

3. Ability to use programmable logical devices, as well as to design analog and digital advanced electronics systems. Ability to design communication devices, such as routers, switches, hubs, transmitters and receivers in different bands.

Transversal:

4. EFFECTIVE USE OF INFORMATION RESOURCES: Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.

5. FOREIGN LANGUAGE: Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

Teaching methodology

- Lectures
- Application classes
- Laboratory activities
- Individual work
- Exercises
- Extended answer test (Final Exam)

Learning objectives of the subject

Learning objectives of the subject:

To understand the general principles and design methods of integrated electronic computing and communication systems.

Learning results of the subject:

- Ability to understand the design process of an integrated circuit.
- Ability to assess the possibilities and limitations of CMOS technology.
- Abitlity to design at circuit level the main subsystems of a digital electronic circuit based on given specifications, including communications applications.
- To acquire knowledge on signal integrity, power consumption and test of an electronic system.

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Study load

Total learning time: 125h	Hours large group:	26h	20.80%
	Hours medium group:	0h	0.00%
	Hours small group:	13h	10.40%
	Guided activities:	0h	0.00%
	Self study:	86h	68.80%

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Content

I: Introduction

Learning time: 4h
Theory classes: 2h
Self study : 2h

Description:
Integrated circuits: presence in communication designs. Trends in communications circuit design. Physical structure of digital integrated circuits.

II. Delay in Digital Circuits

Learning time: 6h
Theory classes: 3h
Self study : 3h

Description:
Delay estimation in Digital Circuits. Maximum working frequency. Data Throughput. Design strategies to increase circuit performances.

III: Power estimation in Digital Circuits.

Learning time: 6h
Theory classes: 3h
Self study : 3h

Description:
Power estimation in digital circuits. Static and dynamic power consumption. Energy - delay trade-off. Design strategies to minimize power consumption. Temperature monitoring in integrated circuits.

IV: Scaling and variability

Learning time: 6h
Theory classes: 3h
Self study : 3h

Description:
Scaling in digital circuits: Moore?s Law and Dennard's scaling rules. Effects of Process-Temperature-Voltage Variations in digital circuits. Design strategies to minimize PVT variations.

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V: New technology challenges.	Learning time: 4h Theory classes: 2h Self study : 2h

Description:
Test of digital circuits. New technologies and technology challenges. More than Moore.

VI: Electronic technology evolution and progress in integrated circuits for data communication.	Learning time: 2h Theory classes: 2h

Description:
Electronic technology evolution and progress in integrated circuits for data communication. Recall of TCP/IP protocol and layers as well as the required main electronic functions at data and network levels: switchers and routers.

VI: INTRODUCTION TO ELECTRONICS FOR COMMUNICATIONS	Learning time: 4h Theory classes: 2h Self study : 2h

Description:
Electronic technology evolution and progress in integrated circuits for data communication. Recall of TCP/IP protocol and layers as well as the required main electronic functions at data and network levels: switchers and routers.

VII: SEMICONDUCTOR MEMORIES	Learning time: 4h Theory classes: 2h Self study : 2h

Description:
Semiconductor memories, advanced FIFO design (queues), queue modeling, system dimensioning. Focus on SRAM 6T cell memories, design, layout, circuits, system.

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VIII: SWITCHERS AND ROUTERS	Learning time: 4h Theory classes: 2h Self study : 2h

Description:
Packet switching. Switch fabric, transmission gate devices. Switch types and design, regular, multi-stage, Clos condition to avoid blocking. Other advanced switcher architectures: with time-slot interchange (TSI), time-space-time (TST), banyan-type, based on direct memory access (DMA).

IX: DATA COMMUNICATION PERIPHERALS AND ARCHITECTURES	Learning time: 4h Theory classes: 2h Self study : 2h

Description:
CRC-circuit implementation. Data communication architectures and protocols: organization into data and control planes. Finite state machines design.

Chapter X: ADVANCED NETWORK PROCESSORS	Learning time: 4h Theory classes: 2h Self study : 2h

Description:
Network processors (NP): motivation, state of the art (Intel, Broadcom, Cisco, Agere, IBM, Motorola, Clearwater, EZchip. Organization, performances.

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Planning of activities

EXERCISES

Description:
Exercises to strengthen the theoretical knowledge.

EXTENDED ANSWER TEST (FINAL EXAMINATION):

Description:
Final examination.

LABORATORY

Hours: 24h
Laboratory classes: 12h
Self study: 12h

Description:
The laboratory part is based on the Xilinx Zynq device: an FPGA with embedded processor. You will use a commercial development board called Zedboard.
The course consists in 4 Labs, the first three are guided and the last one consists on a design proposed by the professor.

Descriptions of the assignments due and their relation to the assessment:
ab 1: Simple embedded design.
Introduction to the design with the Zedboard. Device configuration and simple application program. (2 weeks).

Lab 2: Custom IP design.
You will design a simple IP in the FPGA of the device to be used together with the embedded processor. (2 weeks).

Lab 3: Ethernet configuration.
You will learn how to configure and use the ethernet interface of the device, communicating with the PC. (2 weeks).

Lab 4: Small design.
Proposed by the professor, it usually involves the use of the communications interface available in the Zedboard. Collaboration between teams may be required. (6 weeks).

Qualification system

Final examination: 33%
Partial exams: 14%
Individual assessments: 20%
Laboratory: 33%

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Bibliography

Basic:

Franklin, M.A. [et al.]. Network Processor Design, vol. 3, Issues and practices [en línia] [on line]. Morgan Kaufmann, 2005 [Consultation: 22/06/2017]. Available on: <http://site.ebrary.com/lib/upcatalunya/docDetail.action?docID=10127983>. ISBN 9780120884766.

Weste, N.H.E.; Harris, D.M. CMOS VLSI design: a circuits and systems perspective. 4th ed. Boston: Addison Wesley, 2011. ISBN 9780321547743.

Complementary:

Giladi, R. Network Processors : architecture, programming, and implementation [on line]. Amsterdam: Morgan Kaufmann, 2008 [Consultation: 22/01/2015]. Available on: <http://site.ebrary.com/lib/upcatalunya/docDetail.action?docID=10251232>. ISBN 9780080919591.