

230660 - PROEL - Programmable Electronics

Coordinating unit:	230 - ETSETB - Barcelona School of Telecommunications Engineering
Teaching unit:	710 - EEL - Department of Electronic Engineering
Academic year:	2019
Degree:	MASTER'S DEGREE IN ADVANCED TELECOMMUNICATION TECHNOLOGIES (Syllabus 2019). (Teaching unit Optional) MASTER'S DEGREE IN TELECOMMUNICATIONS ENGINEERING (Syllabus 2013). (Teaching unit Optional) MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2013). (Teaching unit Optional)
ECTS credits:	5
Teaching languages:	English

Teaching staff

Coordinator:	JOAN PONS
Others:	JUAN ANTONIO CHÁVEZ, SANDRA BERMEJO

Degree competences to which the subject contributes

Transversal:

1. **TEAMWORK:** Being able to work in an interdisciplinary team, whether as a member or as a leader, with the aim of contributing to projects pragmatically and responsibly and making commitments in view of the resources that are available.
2. **EFFECTIVE USE OF INFORMATION RESOURCES:** Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.
3. **FOREIGN LANGUAGE:** Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

Teaching methodology

- Lectures
- Laboratory classes
- Group work (distance)
- Short answer test (Control)
- Extended answer test (Final Exam)

Learning objectives of the subject

Learning objectives of the subject:

The aim of this course is the presentation and use of advanced digital design tools and methodologies, with especial emphasis on hardware description languages, programmable logic devices and advanced design techniques for mid-complexity digital subsystems.

Learning results of the subject:

- Ability to design, implement and evaluate mid-complexity digital circuits, using programmable logic devices such as FPGAs and CPLDs.
- Ability to describe and evaluate logic circuits of medium complexity using the VHDL description language and associated tools.
- Knowledge of the features and characteristics of commercial programmable logic devices, such as CPLDs and FPGAs.

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Ability to understand the information provided by the manufacturers.

- Identification and modelling of mid-complex digital systems. Analysis and qualitative approaches, setting methods to validate the results.

Study load

Total learning time: 125h	Hours large group:	13h	10.40%
	Hours medium group:	0h	0.00%
	Hours small group:	26h	20.80%
	Guided activities:	0h	0.00%
	Self study:	86h	68.80%

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Content

<p>1. Introduction to modern digital design</p>	<p>Learning time: 39h Theory classes: 3h Laboratory classes: 10h Self study : 26h</p>
<p>Description:</p> <ul style="list-style-type: none"> - Digital electronic systems, structural & behavioural description, digital ICs and technology alternatives, CAD/CAE tools, design flow. - Programmable logic devices: technologies, performance, mid-complexity (CPLDs, FPGAs) and modern architectures (SoPC). - VHDL description language: basic components, libraries, concurrent and sequential structures, application examples. 	
<p>2. Algorithmic state machines</p>	<p>Learning time: 43h Theory classes: 5h Laboratory classes: 8h Self study : 30h</p>
<p>Description:</p> <ul style="list-style-type: none"> - Specification & design of finite state machines (FSMs). FSM concurrency. - Algorithms and specification of algorithmic state machines (ASMs). Register transfer level description. - ASM data subsystem: components and design. - ASM specific control subsystem design and micro programmed control. 	
<p>3. Advanced design techniques and topics</p>	<p>Learning time: 43h Theory classes: 5h Laboratory classes: 8h Self study : 30h</p>
<p>Description:</p> <ul style="list-style-type: none"> - Power consumption & power estimation. - Metastability. - The synchronous / asynchronous interface. - Time performance estimation. - Clock and reset signal managing. 	

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Planning of activities

LABORATORY

Description:

- Module 1: Introduction to the design software & hardware tools (8h).
- Module 2: VHDL hierarchical design (9h).
- Module 3: ASM design (9h).

ORAL PRESENTATION

Description:

Presentation of a work group.

SHORT ANSWER TESTS (CONTROL)

Description:

Two controls to be done during the course.

EXTENDED ANSWER TEST (FINAL EXAMINATION)

Description:

Final examination.

Qualification system

Final Score: 60% from Theory grade + 40% from Laboratory grade

The Theory grade is the maximum between ...

- 100% from Final examination,
- 50% from Final examination + 50% from partial examinations, controls and other activities done during the course.

Bibliography

Basic:

Balch, M. Complete digital design: a comprehensive guide to digital electronics and computer system architecture. New York: McGraw-Hill, 2003. ISBN 978-0071737708.

Zwolinski, M. Digital system design with VHDL. 2nd ed. Harlow, England: Prentice-Hall, 2004. ISBN 013039985X.

Complementary:

Rushton, A. VHDL for logic synthesis [on line]. 3rd ed. Wiley, 2011 [Consultation: 21/06/2017]. Available on: <<http://onlinelibrary.wiley.com/book/10.1002/9781119995852>>. ISBN 9781119995852.

Lee, S. Advanced digital logic design: using VHDL, state machines, and synthesis for FPGAs. Southbank: Thomson, 2006. ISBN 978-0534466022.