



Course guides

230667 - SCPD - System on Chip Physical Design

Last modified: 29/04/2020

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2013). (Optional subject).
MASTER'S DEGREE IN ADVANCED TELECOMMUNICATION TECHNOLOGIES (Syllabus 2019). (Optional subject).

Academic year: 2020 **ECTS Credits:** 5.0 **Languages:** English

LECTURER

Coordinating lecturer: Moll Echeto, Francesc De Borja
Rubio Sola, Jose Antonio

Others: Moll Echeto, Francesc De Borja
Rubio Sola, Jose Antonio

PRIOR SKILLS

Basic knowledge of CMOS technology and design.
Basic knowledge of digital design, combinational and sequential.

REQUIREMENTS

Graduate studies in Electronic Engineering or equivalent

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:

CEE18. Ability to design CMOS digital and analog integrated circuits of medium complexity.
CEE19. Ability to apply low-power techniques to integrated circuits (ICs).

Transversal:

1. **TEAMWORK:** Being able to work in an interdisciplinary team, whether as a member or as a leader, with the aim of contributing to projects pragmatically and responsibly and making commitments in view of the resources that are available.
2. **EFFECTIVE USE OF INFORMATION RESOURCES:** Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.
3. **FOREIGN LANGUAGE:** Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

TEACHING METHODOLOGY

- Lectures
- Laboratory activities
- Individual work
- Short answer test and exercises (Final Exam)

LEARNING OBJECTIVES OF THE SUBJECT

Learning objectives of the subject:

The aim of this course is to train students in methods of design of CMOS integrated circuits from a high level description to a layout in an efficient way using computers so that the resulting layout satisfies topological, geometric, timing and power-consumption constraints of the design.

Learning results of the subject:

- Ability to understand and apply timing and power constraints to a complex integrated circuit.
- Ability to perform the physical implementation of a complex integrated circuit.
- Ability to apply low power design techniques to integrated circuit design.
- Ability to develop techniques for the design, analysis and evaluation of electronic systems in applications such as automation, aerospace, energy distribution and generation, consumer electronics, biomedicine, etc.
- Ability to analyze, design and evaluate microelectronic integrated circuits.
- Ability to implement advanced design techniques of microelectronic integrated circuits.
- Ability to use state of the art computer aided design (CAD) tools for the design of integrated circuits.

STUDY LOAD

Type	Hours	Percentage
Hours small group	26,0	20.80
Self study	86,0	68.80
Hours large group	13,0	10.40

Total learning time: 125 h

CONTENTS

1. Nanometer chip design overview

Description:

- Challenges in nanometer chip design
- Digital design flows
- Design and verification
- Physical implementation
- Low power design techniques
- Test techniques
- Signoff
- Lab1

Full-or-part-time: 25h

Theory classes: 3h

Laboratory classes: 6h

Self study : 16h



2. RTL synthesis for low power

Description:

- Power problem
- Low power techniques
- Power-aware synthesis (Lab2)

Full-or-part-time: 25h

Theory classes: 3h

Laboratory classes: 4h

Self study : 18h

3. Design planning/floorplanning

Description:

- Low power design flow
- Floorplan
- Power distribution plan
- Lab3

Full-or-part-time: 24h

Theory classes: 2h

Laboratory classes: 4h

Self study : 18h

4. Physical design

Description:

- Placement and optimization
- Clock tree synthesis
- Routing
- Lab4

Full-or-part-time: 27h

Theory classes: 3h

Laboratory classes: 6h

Self study : 18h

5. Sign-off

Description:

- IR drop analysis
- Design finishing and layout verification
- Tapeout
- Lab: project

Full-or-part-time: 6h

Theory classes: 2h

Self study : 4h



6. Design project

Description:

Implement an IP using low power flow.

Full-or-part-time: 18h

Laboratory classes: 6h

Self study : 12h

GRADING SYSTEM

Continuous evaluation (CE):

Partial exams: 25%

Individual assessments: 25%

Laboratory experiences: 50%

Final score: maximum (CE, Final exam)

EXAMINATION RULES.

Final exam: individual

Individual works: Individual

Research presentation: groups of two students

Laboratory: groups of two students

BIBLIOGRAPHY

Complementary:

- Wang, L.T.; Chang, Y.W.; Ting, K. (eds.). Electronic design automation: synthesis, verification, and test. Burlington, MA: Morgan Kaufmann Publishers/Elsevier, 2009. ISBN 9780123743640.

RESOURCES

Other resources:

Slides of the course