Course guide
230735 - HDD - High-Level Digital Design

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree:
MASTER'S DEGREE IN TELECOMMUNICATIONS ENGINEERING (Syllabus 2013). (Optional subject).
MASTER'S DEGREE IN ADVANCED TELECOMMUNICATION TECHNOLOGIES (Syllabus 2019). (Optional subject).
MASTER'S DEGREE IN ELECTRONIC ENGINEERING (Syllabus 2022). (Compulsory subject).

Academic year: 2023  ECTS Credits: 5.0  Languages: English

LECTURER
Coordinating lecturer: Consultar aquí / See here:
https://telecos.upc.edu/ca/estudis/curs-actual/professorat-responsables-coordinadors/responsables-assignatura

Others: Consultar aquí / See here:
https://telecos.upc.edu/ca/estudis/curs-actual/professorat-responsables-coordinadors/professorat-assignat-idioma

PRIOR SKILLS
- Digital design based on an RTL-level hardware description language (VHDL, Verilog, ...).
- Design and simulation of basic digital systems: combinational and sequential logic functions, arithmetic functions and finite state machines.
- Implementation and debugging of basic digital systems on configurable devices (FPGAs).
- Development of software applications based on microprocessor/microcontroller.
- C programming language.

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES
Specific:
CMEE15. Analyze, design and implement hardware/software communication interfaces.
CMEE16. Specify and develop information processing systems using hardware/software co-design techniques.
CMEE17. Design and implement digital systems based on embedded systems (SOC) configurable with high-level description languages and CAE tools.

Transversal:
CTMEE3. Teamwork. Being able to work as a member of an interdisciplinary team, either as a member or carrying out management tasks, in order to contribute to developing projects with pragmatism and a sense of responsibility, assuming commitments taking into account the available resources.

TEACHING METHODOLOGY
- Lectures
- Laboratory classes
- Laboratory practical work
- Collective works (distance)
- Extended answer test (Final Exam)
LEARNING OBJECTIVES OF THE SUBJECT

Learning results of the subject:

- Understand the implications of hardware/software co-design and the use of configurable integrated systems (SOC).
- Design and implement communication interfaces between programmable subsystems (microprocessor/microcontroller) and configurable subsystems (FPGA).
- Understand the high-level design principles of digital systems based on programmable and configurable components.
- Design and implement, using high-level design languages and techniques, digital communication and information processing systems.

STUDY LOAD

<table>
<thead>
<tr>
<th>Type</th>
<th>Hours</th>
<th>Percentage</th>
</tr>
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<tbody>
<tr>
<td>Hours small group</td>
<td>13,0</td>
<td>10.40</td>
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<tr>
<td>Hours large group</td>
<td>26,0</td>
<td>20.80</td>
</tr>
<tr>
<td>Self study</td>
<td>86,0</td>
<td>68.80</td>
</tr>
</tbody>
</table>

Total learning time: 125 h

CONTENTS

1. Introduction

Description:
- Motivation for high-level design
- Principles of hardware/software codesign
- High-level synthesis methodology
- Design optimization principles
- High-level hardware description languages
- Industrial examples

Full-or-part-time: 4h
Theory classes: 2h
Self study: 2h

2. High-level hardware description languages

Description:
- Verilog hardware description language
- SystemVerilog hardware description language
- SystemC hardware description language
- Design verification based on SystemVerilog

Full-or-part-time: 18h
Theory classes: 8h
Self study: 10h
3. High-level digital synthesis

Description:
- Bit accurate data types
- Principles of high-level synthesis
- Scheduling
- Resource allocation
- Loop unrolling
- IO and memories

Full-or-part-time: 12h
Theory classes: 6h
Self study : 6h

4. Hardware/software interfaces

Description:
- Principles of hardware/software communication
- On-chip buses
- Microprocessor interfaces
- Hardware interfaces

Full-or-part-time: 8h
Theory classes: 2h
Self study : 6h

5. Design of custom processing systems

Description:
- Video subsystems
- Vector and matrix multiplication
- Sorting algorithms

Full-or-part-time: 24h
Theory classes: 4h
Self study : 20h

LABORATORY

Description:
- Design of a software application for the programmable section of a SOC
- Development of custom peripherals and interrupt management
- Introduction to the SystemVerilog language and to the QuestaSim simulator
- Design of an arithmetic co-processor
- Design and implementation of an AXI4 interface for the arithmetic co-processor
- Introduction to the high-level design and synthesis tool
- High-level design of a signal processing system
- Custom project

Full-or-part-time: 26h
Laboratory classes: 13h
Self study : 13h
**ACTIVITIES**

**LABORATORY**

Full-or-part-time: 26h  
Theory classes: 13h  
Self study: 13h

**COLLECTIVE WORK**

Description:  
A collective (2-3 people) work on one of the topics suggested in chapter 5. The workgroup should deliver a presentation and a written report and should provide an oral presentation.

Full-or-part-time: 24h  
Theory classes: 4h  
Self study: 20h

**EXTENDED ANSWER TEST (FINAL EXAMINATION)**

Description:  
Final examination.

Full-or-part-time: 2h 30m  
Theory classes: 2h 30m

**GRADING SYSTEM**

Final exam: 40%  
Collective works: 20%  
Laboratory assessment: 40%

**BIBLIOGRAPHY**

**Basic:**


**Complementary:**