Course guides
270616 - AVLSI - Algorithms for VLSI

Unit in charge: Barcelona School of Informatics
Teaching unit: 723 - CS - Department of Computer Science.
Degree: MASTER’S DEGREE IN INNOVATION AND RESEARCH IN INFORMATICS (Syllabus 2012). (Optional subject).
Academic year: 2020
ECTS Credits: 6.0
Languages: English

LEXCUTER

Coordinating lecturer: JORDI CORTADELLA FORTUNY
Others: Primer quadrimestre: JORDI CORTADELLA FORTUNY - 10

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
CEE3.1. Capability to identify computational barriers and to analyze the complexity of computational problems in different areas of science and technology as well as to represent high complexity problems in mathematical structures which can be treated effectively with algorithmic schemes.
CEE3.2. Capability to use a wide and varied spectrum of algorithmic resources to solve high difficulty algorithmic problems.
CEE3.3. Capability to understand the computational requirements of problems from non-informatics disciplines and to make significant contributions in multidisciplinary teams that use computing.

Gnerical:
CG1. Capability to apply the scientific method to study and analyse of phenomena and systems in any area of Computer Science, and in the conception, design and implementation of innovative and original solutions.
CG3. Capacity for mathematical modeling, calculation and experimental designing in technology and companies engineering centers, particularly in research and innovation in all areas of Computer Science.

Transversal:
CTR6. REASONING: Capacity for critical, logical and mathematical reasoning. Capability to solve problems in their area of study. Capacity for abstraction: the capability to create and use models that reflect real situations. Capability to design and implement simple experiments, and analyze and interpret their results. Capacity for analysis, synthesis and evaluation.

Basic:
CB6. Ability to apply the acquired knowledge and capacity for solving problems in new or unknown environments within broader (or multidisciplinary) contexts related to their area of study.
CB8. Capability to communicate their conclusions, and the knowledge and rationale underpinning these, to both skilled and unskilled public in a clear and unambiguous way.
CB9. Possession of the learning skills that enable the students to continue studying in a way that will be mainly self-directed or autonomous.

TEACHING METHODOLOGY

The theoretical content of the course is taught in the theory lectures. During the practical classes, practical examples are solved and different types of problems are proposed. These problems will have to be solved during the time of autonomous learning. An algorithmic project will also be proposed during the course. Students will have to solve and implement it during their time of autonomous learning.

LEARNING OBJECTIVES OF THE SUBJECT
STUDY LOAD

<table>
<thead>
<tr>
<th>Type</th>
<th>Hours</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hours small group</td>
<td>12,0</td>
<td>8.00</td>
</tr>
<tr>
<td>Hours medium group</td>
<td>12,0</td>
<td>8.00</td>
</tr>
<tr>
<td>Guided activities</td>
<td>6,0</td>
<td>4.00</td>
</tr>
<tr>
<td>Self study</td>
<td>96,0</td>
<td>64.00</td>
</tr>
<tr>
<td>Hours large group</td>
<td>24,0</td>
<td>16.00</td>
</tr>
</tbody>
</table>

Total learning time: 150 h

CONTENTS

Introduction.
Description:
Integrated circuit fabrication. Layout layers and design rules. VLSI design flow. VLSI design styles.

Two-level logic synthesis
Description:

Multi-level logic synthesis
Description:
Kernel-based algebraic decomposition. AIG-based decomposition. Technology mapping for standard cells and FPGAs.

Formal verification
Description:

Partitioning and Floorplanning
Description:

Placement
Description:
## Global routing

**Description:**

## Detailed routing

**Description:**

## ACTIVITIES

### Learning the design flow of a VLSI circuit

**Full-or-part-time:** 4h
- Theory classes: 2h
- Self study: 2h

### Learning of algorithms for logic synthesis

**Full-or-part-time:** 34h
- Theory classes: 10h
- Practical classes: 4h
- Self study: 20h

### Learning of techniques for formal verification of circuits

**Full-or-part-time:** 24h
- Theory classes: 6h
- Practical classes: 4h
- Self study: 14h

### Learning of techniques for circuit floorplanning and placement

**Full-or-part-time:** 32h
- Theory classes: 8h
- Practical classes: 4h
- Self study: 20h

### Learning of routing algorithms

**Full-or-part-time:** 32h
- Theory classes: 10h
- Practical classes: 6h
- Self study: 16h
GRADING SYSTEM

Grade = 40% FW + 30% FT + 20% EX + 10% SP

FW = Final Work (graded from 0 to 10) in which each participant is required to present a research paper or section of a book (previously assigned by the lecturer). The presentation consists of:
* 3-5 minutes background on the topic of the paper, a motivation.
* 1 minute overview of the key ideas of the paper.
* 15 minutes presentation with most important details.
* 5 minutes demo of a program that implements the ideas introduced in the paper.

FT = Final test graded from (0 to 10) including all the contents of course.

EX = Exercises assigned to the student and solved during the Autonomous Learning time

SP = Summaries and participation (graded from 0 to 10) in which each participant is required to deliver a summary (1 page extent) of each others presentation and to participate (with questions and comments).

BIBLIOGRAPHY

Basic: