270640 - MA - Multiprocessors Architecture

Coordinating unit: 270 - FIB - Barcelona School of Informatics
Teaching unit: 701 - AC - Department of Computer Architecture
Academic year: 2018
Degree: MASTER'S DEGREE IN INNOVATION AND RESEARCH IN INFORMATICS (Syllabus 2012). (Teaching unit Optional)
ECTS credits: 6
Teaching languages: Catalan

Degree competences to which the subject contributes

Basic:
CB9. Possession of the learning skills that enable the students to continue studying in a way that will be mainly self-directed or autonomous.

Specific:
CEE4.1. Capability to analyze, evaluate and design computers and to propose new techniques for improvement in its architecture.

General:
CG1. Capability to apply the scientific method to study and analyse of phenomena and systems in any area of Computer Science, and in the conception, design and implementation of innovative and original solutions.

Transversal:
CTR5. APPROPRIATE ATTITUDE TOWARDS WORK: Capability to be motivated by professional achievement and to face new challenges, to have a broad vision of the possibilities of a career in the field of informatics engineering. Capability to be motivated by quality and continuous improvement, and to act strictly on professional development. Capability to adapt to technological or organizational changes. Capacity for working in absence of information and/or with time and/or resources constraints.

Teaching methodology

Teaching methodology is described in Activities

Learning objectives of the subject

Study load

<table>
<thead>
<tr>
<th>Total learning time: 150h</th>
<th>Theory classes: 27h</th>
<th>18.00%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Practical classes: 9h</td>
<td>6.00%</td>
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</tr>
<tr>
<td>Laboratory classes: 9h</td>
<td>6.00%</td>
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</tr>
<tr>
<td>Guided activities: 9h</td>
<td>6.00%</td>
<td></td>
</tr>
<tr>
<td>Self study: 96h</td>
<td>64.00%</td>
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**Content**

**Program**

**Degree competences to which the content contributes:**

**Description:**
1. Introduction to multiprocessor architecture
2. MP Software and ISA
3. Cores and micro-architecture support for MPs
4. Memory hierarchy in MPs
5. Coherency and Consistency
6. Interconnection Networks (on and off-die)
7. Client vs Server SMPs
8. CMPs
9. Clusters
10. SIMD systems
11. Massively Parallel MPs
12. Heterogeneous systems
13. GPGPU, FPGAs

**Qualification system**

Not yet translated

**Bibliography**

**Basic:**
