270646 - PD - Processor Design

Coordinating unit: 270 - FIB - Barcelona School of Informatics
Teaching unit: 701 - DAC - Department of Computer Architecture
Academic year: 2019
Degree: MASTER'S DEGREE IN INNOVATION AND RESEARCH IN INFORMATICS (Syllabus 2012). (Teaching unit Optional)
ECTS credits: 6
Teaching languages: English

Teaching methodology

The main concepts of processor architecture will be introduced in the lectures. In the interactive problem-solving classes the students will participate into applying the concepts learned into real world designs. Finally, the students will complete their learning experience with the lab sessions where they will put in practice the concepts learned in the lectures and applied in the problem-solving classes.

Learning objectives of the subject

1. To understand and implement a simple pipelined processor.
2. To program skillfully in a hardware description language
3. To understand the intricacies of advanced microprocessor structures such as the memory hierarchy, branch prediction, out-of-order execution and multithreading (among other).

Study load

<table>
<thead>
<tr>
<th>Total learning time: 150h</th>
<th>Hours large group: 24h</th>
<th>16.00%</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Hours medium group: 12h</td>
<td>8.00%</td>
</tr>
<tr>
<td></td>
<td>Hours small group: 12h</td>
<td>8.00%</td>
</tr>
<tr>
<td></td>
<td>Guided activities: 6h</td>
<td>4.00%</td>
</tr>
<tr>
<td></td>
<td>Self study: 96h</td>
<td>64.00%</td>
</tr>
</tbody>
</table>
### Content

#### Historical Perspective

**Degree competences to which the content contributes:**

**Description:**
Description of how processor design has evolved through the technology changes from mechanical devices to the current FinFET transistors.

#### Technology-Aware Processor Design

**Degree competences to which the content contributes:**

**Description:**
Introduction to the quantification and evaluation of technology-related metrics such as area, power and timing.

#### Processor Design Cycle and Fabrication

**Degree competences to which the content contributes:**

**Description:**
Description of the VLSI Design stages including an introduction to placement and routing techniques.

#### Memory Hierarchy

**Degree competences to which the content contributes:**

**Description:**
Introduction to the efficient construction of on-chip memory structures. Design choices. Performance and power consumption.

#### Modern Processor Architectures

**Degree competences to which the content contributes:**

**Description:**
Description and implementation of state-of-the-art processor architectures such as superscalar, multithreading or chip-multiprocessors.
Planning of activities

<table>
<thead>
<tr>
<th>Design and Simulation Tools</th>
<th>Hours: 0h</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Theory classes: 0h</td>
</tr>
<tr>
<td></td>
<td>Practical classes: 0h</td>
</tr>
<tr>
<td></td>
<td>Laboratory classes: 0h</td>
</tr>
<tr>
<td></td>
<td>Guided activities: 0h</td>
</tr>
<tr>
<td></td>
<td>Self study: 0h</td>
</tr>
</tbody>
</table>

Description:
First contact with the circuit design and simulation tools. Introduction to the basic functionalities and components needed to implement a simple microprocessor.

Specific objectives:
1, 2

Qualification system
The course has three marks:
1) Lab sessions (Lab)
2) Presentation of a research topic (T)

The final mark will be computed as: 0,8 x Lab + 0,2 T

Bibliography
Basic:

