Course guide
320098 - ED - Digital Electronics

Last modified: 19/04/2023

Unit in charge: Terrassa School of Industrial, Aerospace and Audiovisual Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: BACHELOR'S DEGREE IN AUDIOVISUAL SYSTEMS ENGINEERING (Syllabus 2009). (Compulsory subject).

Academic year: 2023 **ECTS Credits:** 6.0 **Languages:** Catalan, Spanish

LECTURER

Coordinating lecturer: JUAN MON GONZÁLEZ

Others: MONTSERRAT CORBALAN FUERTES

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
CE14-ESAUD. Ability to analyze and design combinational and sequential circuits, synchronous and asynchronous, and to use microprocessors and integrated circuits. (Common module for the telecommunications branch)
CE15-ESAUD. Knowledge and application of the fundamentals of hardware description languages. (Common module for the telecommunications branch)

Generical:
CG03-ESAUD. Knowledge of basic subjects and technologies, which enables learning of new methods and technologies, as well as providing great versatility to adapt to new situations.
CG04-ESAUD. Ability to solve problems with initiative, decision-making, creativity, and to communicate and transmit knowledge, skills, and abilities, understanding the ethical and professional responsibility of the Technical Telecommunications Engineer's activity.
CG05-ESAUD. Knowledge for the realization of measurements, calculations, valuations, appraisals, expert opinions, studies, reports, task planning, and other similar work in their specific field of telecommunications.

TEACHING METHODOLOGY

Directed learning hours include large group lectures in which the lecturer briefly presents the general learning objectives related to the basic concepts of the subject. The lecturer then uses practical exercises to motivate and encourage students to participate actively in their learning. Digital support material is available through the ATENEA virtual campus and includes learning objectives by content, concepts, examples, assessment programming, directed learning and bibliographies. Directed learning hours also include problem solving sessions (medium-sized groups) in which students work in groups of 3 or 4 on exercises and problems related to specific learning objectives of each of the course contents. These sessions aim to develop generic competencies such as teamwork by using cooperative learning methods in the classroom. The last type of directed learning hours consists of four laboratory practicals in which students work in pairs to develop basic skills associated with designing, simulating and implementing digital circuits using CAD tools. Students will also be taught how to apply the laboratory electronic design method. Other self-directed learning activities include directed reading, problem solving and completing self-learning questionnaires using the ATENEA virtual campus.

LEARNING OBJECTIVES OF THE SUBJECT

Teach students the theory behind the conception and design of digital systems. Familiarise students with CAD tools for digital system design and teach them how to implement them using programmable logic devices. Students will also be taught how to use the VHDL hardware description language, microprocessors and integrated circuits. This subject also aims to develop specific and transversal competencies associated with the coursework, as detailed below.

STUDY LOAD

Type	Hours	Percentage
Hours large group	15,0	10.00
Hours medium group	30,0	20.00
Hours small group	15,0	10.00
Self study	90,0	60.00

Total learning time: 150 h

CONTENTS

Topic 1: INTRODUCTION TO LOGIC CIRCUITS

Description:
- Basic logic operations
- Analysis of logic circuits
- Logic gate synthesis
- Integrated circuit technology
- Standard integrated circuits
- Programmable logic devices

Related activities:
Problem-based lectures
Activity 1 and activity 2 are carried out. Activity 1 is an individual continuous assessment test to be completed outside class hours. The description and materials are available on the Atenea digital campus. Activity 2 is a directed practical laboratory exercise.

Full-or-part-time: 17h
Theory classes: 2h
Practical classes: 4h
Laboratory classes: 2h
Self study : 9h

Topic 2: PROGRAMMABLE LOGIC DEVICES AND VHDL

Description:
- Low- and high-density programmable logic: PLDs and FPGAs.
- Introduction to VHDL: entities, architectures, packets and libraries.

Related activities:
Problem-based lectures
Activity 2 is carried out. Activity 2 is a directed practical laboratory exercise.

Full-or-part-time: 17h
Theory classes: 2h
Practical classes: 4h
Laboratory classes: 2h
Self study : 9h

Topic 3: COMBINATIONAL LOGIC SYSTEMS

Description:
- Combinational arithmetic circuits (adders, subtractors and comparators) and numeration systems
- Arithmetic circuit design in VHDL
- Multiplexers
- Decoders/Demultiplexers
- Encoders
- Combinatorial block design in VHDL

Related activities:
Problem-based lectures
Activity 2 and activity 3 are carried out. Activity 2 is a directed practical laboratory exercise.
Activity 3 is a problem-solving exercise.

Full-or-part-time: 37h
Theory classes: 4h
Practical classes: 7h
Laboratory classes: 4h
Self study : 22h

Topic 4: SEQUENTIAL LOGIC SYSTEMS

Description:
- Flip-Flops (D flip-flop, T flip-flop and JK flip-flop)
- Registers (shift registers, Enable entry registers)
- Register design in VHDL
- Counters (asynchronous and synchronous)
- Counter design in VHDL

Related activities:
Problem-based lectures
Activity 1 is carried out. Activity 1 is an individual continuous assessment test to be completed outside class hours. The description and materials are available on the Atenea digital campus. Activity 2 is a directed practical laboratory exercise.

Full-or-part-time: 35h
Theory classes: 3h
Practical classes: 7h
Laboratory classes: 5h
Self study : 20h

Topic 5: SYNCHRONOUS SEQUENTIAL CIRCUITS

Description:
- Finite-state machines (FSMs)
- Moore model and Mealy model
- Synthesis of synchronous sequential circuits (state diagram and state transition table)
- Finite-state machine design in VHDL

Related activities:
Problem-based lectures
Activity 2 and activity 3 are carried out. Activity 2 is a directed practical laboratory exercise. Activity 3 is a problem-solving exercise.

Full-or-part-time: 44h
Theory classes: 4h
Practical classes: 8h
Laboratory classes: 2h
Self study : 30h

ACTIVITIES

CONTINUOUS ASSESSMENT TEST (TOPIC 1, 3 AND 4)

Description:
Making individual autocorrect quizzes outside the classroom available in ATENEA with limited time and number of attempts. The questions and their order changes randomly, there are a database with different questions. In case of multiple-choice questions, the options also change randomly. Subsequently, the teacher reviews the qualifications and makes a general reflection in the classroom about common mistakes in order to clarify the main concepts of this activity.

Specific objectives:
After the activity, the student should be able to:
- Represent numbers in binary, octal and hexadecimal.
- Convert between decimal, binary, octal and hexadecimal number systems.
- Perform arithmetic operations in the binary system.
- Analyze and synthesize logic circuits.
- Know the basic devices for implementing sequential logic systems.
- Learn the most commonly used sequential blocks and applications.
- Analyze and synthesize digital circuits using sequential building blocks.

Material:
Lectures note an exercise collection. Quizzes with different types of questions, multiple choice and short answer, available in ATENA.

Delivery:
The quizzes are available in the digital campus ATENEA. The questionnaire results represent 5% of the final mark.

Full-or-part-time: 1h
Theory classes: 1h

LAB ASSIGNMENTS (TOPIC 1, 2, 3, AND 4)

Description:
The Lab sessions involve teams of two students. In these sessions, the students will carry out the design, simulation and implementation of combinational and sequential circuits using CAD tools for designing digital circuits. The students have to do a Pre-Lab report as autonomous learning before the lab session.

Specific objectives:
At the end of each lab session, the student should be able to:
- Design, simulate and implement combinational and sequential logic circuits designs on state-of-the-art Programmable Logic Devices.

Material:
Tutorial and documentation about software and hardware platform used in the laboratory and the laboratory assignments. The laboratory assignments and supporting documentation is available in the digital campus ATENEA.

Delivery:
The Pre-Lab report and the Lab report can be required. The Pre-Lab and Lab reports are delivered by the digital campus ATENEA and represent 30% of the final mark.

Full-or-part-time: 25h
Laboratory classes: 15h
Self study: 10h

PROBLEM SOLVING TEAM (TOPIC 3 AND 5)

Description:
Students outside the classroom prepare different exercises proposed in ATENEA, where they have to apply specific learning objectives with the related topics.

Specific objectives:
At the end of these activities, the student should be able to:
- Analyze and synthesize digital circuits using combinational blocks.
- Analysis and synthesis of synchronous sequential digital circuits.
- Understand the operation of a microprocessor-based system.

Material:
Exercise collection. The student may bring all the theoretical material that he thinks it is needed.

Delivery:
The exercise solutions are delivered through digital campus ATENEA. The exercise solutions represent 5% of the final mark.

Full-or-part-time: 14h
Practical classes: 4h
Self study: 10h

FIRST-SEMESTER EXAMINATION (TOPIC 1, 2, AND 3)

Description:
Single Test in classroom solving different problems related to learning objectives of the subject contents to the first- semester (2h 30min).

Specific objectives:
After the exam, the student should be able to:
- Represent and perform arithmetic on numbers in the binary system.
- Analyze and synthesize combinational logic circuits.

Material:
Exam.

Delivery:
Exam solution. The solution of the exam represents 25% of the final mark.

Full-or-part-time: 9h
Theory classes: 3h
Self study: 6h

SECOND-SEMESTER EXAMINATION (TOPIC 3, 4, AND 5)

Description:
Single Test in classroom solving different problems related to learning objectives of the subject contents to the second-semester (2h 30m).

Specific objectives:
After the exam, the student should be able to:
-Analyze and design combinational and sequential circuits, synchronous and asynchronous.
- Know and apply the different technologies of integrated circuits.

Material:
Exam.

Delivery:
Exam solution. The solution of the exam represents 35% of the final mark.

Full-or-part-time: 9h
Theory classes: 3h
Self study: 6h

GRADING SYSTEM

Oral and written exams 60% (25% First-semester examination, 35% Second-semester examination).
Laboratory sessions 30%.
Other Delivery Questionnaires and Solve exercises) 10%.
For those students who meet the requirements and submit to the reevaluation examination, the grade of the reevaluation exam will replace the grades of all the on-site written evaluation acts (tests, midterm and final exams) and the grades obtained during the course for lab practices, works, projects and presentations will be kept.
If the final grade after reevaluation is lower than 5.0, it will replace the initial one only if it is higher. If the final grade after reevaluation is greater or equal to 5.0, the final grade of the subject will be pass 5.0.

BIBLIOGRAPHY

Basic:
- Floyd, Thomas L. Fundamentos de sistemas digitales [on line]. 11ª ed. Madrid: Pearson Educación, 2016 [Consultation: 19/09/2022]. Available on: https://www-ingebook-com.recursos.biblioteca.upc.edu/ib/NPcd/IB_BooksVis?cod_primaria=1000187&codigo_libro=6120.
- Stephen, Brown; Zvonko, Vranesic. Fundamentos de lógica digital con diseño VHDL. 2ª ed. México DF: McGraw-Hill, 2006. ISBN 9701056094.

Complementary:
- Wakerly, John F. Diseño digital: principios y prácticas. 3ª ed. México: Pearson Educación, 2001. ISBN 9789702607205.

RESOURCES

Other resources:
-Lecture notes available in the virtual campus ATENEA.